

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- ✓ TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

MEMBRANE DIELECTRIC ISOLATION IC FABRICATION

Glenn J. Leedy

BACKGROUND OF THE INVENTION

Field of the Invention

5 This invention relates to methods for fabricating integrated circuits on and in flexible membranes, and to structures fabricated using such methods.

Description of Related Art

Mechanically and thermally durable free standing dielectric and semiconductor membranes have been disclosed with thicknesses of less than 2 μm . (See commonly invented U.S. Patent No. 4,924,589, and U.S. patent application Serial No. 07/482,135, filed February 16, 1990, now U.S. Patent No. 5,103,557, both incorporated herein by reference). This disclosure combines the novel use of these technologies and other integrated circuit (IC) processing techniques to form ICs as membranes typically less than 8 μm thick. This approach to IC fabrication falls under the generic industry-established title known as Dielectric Isolation (DI), and is inclusive of subject areas such as Silicon-on-Insulator (SOI) and Silicon-on-Sapphire (SOS). ICs formed from dielectric and semiconductor membranes can reduce significantly the number and complexity of processing steps presently used to provide complete IC device isolation; dielectric isolation techniques that provide dielectric isolation on all surfaces of the individual circuit devices comprising the complete IC are not as yet widely used in volume IC fabrication. Integrated Circuits are defined as commonly understood today when referring to SSI, MSI, LSI, VLSI, ULSI, etc. levels of circuit complexity.

LUMINOSITY APPENDIX

SUMMARY OF THE INVENTION

This invention is directed to a general method for the fabrication of integrated circuits and interconnect metallization structures from membranes of dielectric and 5 semiconductor materials. The fabrication technology in accordance with this invention is referred to herein as Membrane Dielectric Isolation (MDI), and the circuits made from it as circuit membranes. The novel use of materials and processing techniques provides for the fabrication of 10 high temperature, mechanically durable, large area free standing membranes (greater than 1 square cm in area) from low stress dielectric and/or semiconductor films. These membranes permit the application (continued use) of most of the established integrated processing methods for the 15 fabrication of circuit devices and interconnect metallization.

In accordance with the invention, an integrated circuit is formed on a tensile low stress dielectric membrane comprised of one layer or a partial layer of 20 semiconductor material in which are formed circuit devices and several layers of dielectric and interconnect metallization. Also, a structure in accordance with the invention is a tensile membrane of semiconductor material in which are formed circuit devices with multiple layers 25 of tensile low stress dielectric and metallization interconnect on either side of the semiconductor membrane.

The membrane structure is a processing or manufacturing structure for enabling the manufacture of novel and more cost effective integrated circuits. This 30 is in addition to an objective to manufacture an integrated circuit, or portion thereof, in a membrane or thin film form.

The general categories of circuit membranes that can be made by this invention are:

- 35 1. Large scale dielectric isolated integrated

circuits formed on or from semiconductor or non-semiconductor substrates.

2. Multi-layer interconnect metallization circuits formed on or from semiconductor or non-semiconductor substrates.

The primary objectives of the MDI fabrication technology disclosed herein are the cost effective manufacture of high performance, high density integrated circuits and integrated circuit interconnect with the elimination or reduction of detrimental electrical effects on the operation of individual circuit devices (e.g. diodes, transistors, etc.) by completely isolating with a dielectric material each such circuit device from the common substrate upon which they are initially fabricated, and therefore, from each other, and to provide a more versatile and efficient physical form factor for the application of integrate circuits. Some of the benefits of the MDI IC fabrication process are the elimination or reduction of substrate current leakage, capacitive coupling and parasitic transistor effects between adjoining circuit devices. The MDI IC fabrication process benefits extend to several other categories of IC fabrication such as lower IC processing costs due to fewer IC isolation processing steps, greater IC transistor densities through the capability to use established IC processing techniques to fabricate interconnect metallization on both sides of a MDI IC circuit membrane, and greater IC performance through novel transistor structures.

30 The strength of the MDI processes is primarily drawn from two areas:

(1) The ability to make a large area flexible thin film free standing dielectric membrane, typically framed or suspended or constrained at its edges by a substrat frame or ring, or bonded frame or ring. This membrane is

able to withstand a wide range of IC processing techniques and processing temperatures (of at least 400°C) without noticeable deficiency in performance. The present dielectric materials that meet these requirements are 5 silicon dioxide and silicon nitride films when prepared with specific low stress film deposition recipes for instance on equipment supplied by Novellus Systems, Inc. Dielectric free standing films created by CVD process methods such as silicon carbide, boron nitride, boron 10 carbon nitride aluminum oxide, aluminum nitride, tantalum pentoxide, germanium nitride, calcium fluoride, and diamond have been produced, and can potentially be used as one of the dielectric materials in a MDI circuit membrane when deposited at an appropriate level of surface stress. 15 Advances in the technology for making low stress dielectric films will likely produce additional free standing films that can be used as described herein.

(2) The ability to form a uniform thin film single crystal semiconductor substrate either as the primary 20 substrate of semiconductor devices or as a carrier substrate upon which semiconductor devices could be grown epitaxially. Several methods toward this end are disclosed herein, and other techniques which are modifications thereof exist. Further, in certain 25 applications polycrystalline semiconductor membranes such as polysilicon can be used in substitution for monocrystalline material.

It is the combination of the use of low stress free standing dielectric films with the appropriate processing 30 qualities and membrane or thin film single crystalline (monocrystalline), polycrystalline or amorphous semiconductor substrate formation that provides much of the advantage of the MDI IC fabrication process. The following methods are encompassed within the present 35 disclosure:

1. Methods for the fabrication of low stress free standing (thin film) dielectric membranes that encapsulate each semiconductor device that comprises an IC.
- 5 2. Methods for the formation of uniform thickness semiconductor membrane (thin film) substrates for use in combination with low stress dielectric materials.
- 10 3. Methods for the fabrication of semiconductor devices within and on a dielectric membrane that comprises a circuit membrane.
4. Methods for the formation of interconnect metallization structures within and on a dielectric membrane that comprises a circuit membrane.
- 15

The MDI circuit fabrication process in one embodiment starts with a semiconductor wafer substrate, and results in an IC in the form of a circuit membrane where each transistor or semiconductor device (SD) in the IC has complete dielectric isolation from every other such semiconductor device in the IC. Only interconnect at the specific electrode contact sites of the semiconductor devices provides electrical continuity between the semiconductor devices. The primary feature of the MDI process is complete electrical isolation of all semiconductor devices of an IC from all of the intervening semiconductor substrate on which or in which they were initially formed and to do so at lower cost and process complexity than existing bulk IC processing methods.

Other features of the MDI process are vertical electrode contact (backside interconnect metallization), confined lateral selective epitaxial growth, non-symmetric dopant profiles, and the use of a MDI circuit membrane to serve as a conformal or projection mask for lithography processing. Even if the initial substrate with which MDI

processing begins with is the most commonly used semiconductor silicon, the resulting IC need not be composed of silicon-based devices, but could be of any semiconductor device material such as GaAs, InP, HgCdTe, 5 InSb or a combination of technologies such as silicon and GaAs grown on a silicon substrate through epitaxial means. Silicon is an inexpensive and well understood semiconductor substrate material with superior mechanical handling properties relative to most other presently 10 established semiconductor materials. The MDI process is not limited to starting with a silicon substrate and the process definition of MDI is not dependent on use of silicon; however, there are presently clear advantages to using silicon as a starting semiconductor substrate, and 15 the chief embodiment disclosed herein of MDI uses a starting semiconductor substrate material of silicon.

The benefits to fabricating an IC with the MDI process are significant over prior art methods, some of these benefits being:

- 20 1. Complete electrical isolation of semiconductor devices.
2. Vertical semiconductor device structures.
3. Lower processing costs through lower processing complexity or fewer device isolation processing steps.
- 25 4. Conformal mask lithography through the membrane substrate.
5. Control of depth of focus during lithography exposure due to control of substrate thickness.
- 30 6. Application of interconnect metallization to both sides of the IC.
7. Through-membrane (substrate) interconnect metallization routing.
8. Three dimensional IC structures through the bonding of circuit membrane IC layers.

9. Efficient conductive or radiant cooling of IC components of circuit membrane.
10. Direct optical (laser) based communication between parallel positioned membrane ICs.
- 5 11. Higher performance ICs.
12. Vertical semiconductor device structure formation.
13. Novel selective epitaxial device formation.

In some semiconductor technologies it is not necessary to have complete isolation between each transistor or semiconductor device, such as certain applications using polycrystalline or amorphous TFTs (thin film transistors). This is not a limitation on the MDI process, because semiconductor device side wall isolation is an option in the MDI process. What is novel is that the MDI process provides general methods by which thin films or membranes of dielectric and semiconductor materials can be formed into a free standing IC or circuit membrane.

20 BRIEF DESCRIPTION OF THE FIGURES

Figures 1a to 1j show a dielectric and semiconductor membrane substrate in cross-section.

Figure 2 shows an etched silicon substrate membrane in cross-section.

25 Figures 3a, 3b show dielectric membranes with semiconductor devices.

Figure 4 shows an alignment mark of a circuit membrane in cross-section.

Figure 5 shows support structures for a membrane structure isolation structure.

Figure 6a to 6i show a circuit membrane Air Tunnel structure.

Figure 7 shows stacked circuit membranes with optical input/output.

Figure 8 shows a three dimensional circuit membrane.

Figures 9a to 9j show fabrication of a MOSFET in a membrane.

Figures 10a to 10d show fabrication of a transistor 5 by lateral epitaxial growth on a membrane.

Figures 11a to 11f show vertical MOSFET and bipolar transistors formed on a membrane.

Figure 12a to 12g show transistor fabrication on a membrane using confined laterally doped epitaxy.

10 Figures 12h to 12j show cross-sections of selective epitaxial growth on a membrane.

Figures 13a to 13d show cross-sections of multi-chip modules.

Figure 14 shows a cross-section of a membrane formed 15 on a reusable substrate.

Figure 15 shows a cross-section of the membrane of Figure 14 with a support frame attached.

Figures 16a, 16b show multi-chip modules in packages.

Figures 17a to 17c show soldering of bond pads of a 20 circuit membrane to a die.

Figure 18 shows bond pads on a die.

Figures 19a, 19b show bonding and de-bonding of a die to a circuit membrane.

Figures 20, 21 show two sides of a circuit membrane.

25 Figures 22a to 22c show formation of a metal trace in a circuit membrane by a lift-off process.

Figures 23a, 23b show use of a buried etch stop layer to form a circuit membrane having a thinner inner portion.

Figures 24, 25 show a source-integrated light valve 30 for direct write lithography.

Figures 26, 27 are cross-sections of X-ray sources for the device of Figures 24, 25.

Figures 28a to 28b show a coil for the device of Figure 24.

35 Figures 29a to 29k show portions of a source-external

radiation valve for direct write lithography device.

Figures 29l to 29p show use of fixed freestanding membrane lithography masks.

Figure 30 shows a cross-section of a lithographic tool.

Figures 31a to 31c show cross-sections of a display formed on a membrane.

Figures 32a, 32b show bonding of two circuit membranes.

10 DETAILED DESCRIPTION OF THE INVENTION

The MDI process is the formation of an IC or interconnect metallization circuit as a free standing dielectric and/or semiconductor circuit membrane. Each semiconductor device comprising an IC circuit membrane is 15 a semiconductor device optionally isolated from adjoining semiconductor devices, and where each semiconductor device is formed on or in a membrane of semiconductor material typically less than 8 μm in thickness. The overall thickness of a circuit membrane is typically less than 20 50 μm and preferably less than 8 μm . The dielectric membrane is compatible with most higher temperature IC processing techniques.

MDI Fabrication Process

Several process variations can be used to form the 25 thin film or membrane of semiconductor material for use in the MDI process. Additional related methods for forming semiconductor membranes may exist or come into existence and are included in the MDI technology.

Examples of some of the methods that can be used for 30 forming silicon single crystal thin films are:

1. Heavily boron doped (typically greater than 10^{17} atoms/cm²) etch stop layer (formed by diffusion, implant or epitaxy) with optional epitaxial SiGe (less than 20% Ge)

anti-autodoping overlayer layer and optional epitaxial layer.

2. O₂ (oxide) and N₂ (Nitride) implant etch stop barrier layer. Implant concentrations are typically 5 between 10 to 100 times less for formation of an etch stop barrier layer than that required to form a buried oxide or nitride dielectric isolation layer as presently done with a standard thickness silicon substrate.

3. Buried oxide etch stop barrier layer formed from 10 a porous silicon layer.

4. High precision double sided polished substrate and masked timed chemical etch back of back-side.

5. Electro-chemical etch stop.

6. Buried etch stop layer formation through anodic 15 or thermal wafer bonding in combination with precision substrate polishing and chemical etching.

There are many established methods for forming thin semiconductor substrates or membranes. The MDI process requires that the semiconductor membrane forming process 20 (thinning process) produce a highly uniform membrane typically less than 2 μm thick and that the surface tension of the semiconductor membrane be in low tensile stress. If the membrane is not in tensile stress, but in compressive stress, surface flatness and membrane 25 structural integrity will in many cases be inadequate for subsequent device fabrication steps or the ability to form a sufficiently durable free standing membrane.

The use of highly doped layers on the surface or near the surface of the substrate formed by diffusion, implant 30 or epitaxial means is an established method for forming a barrier etch stop layer. A heavily doped boron layer will etch 10 to 100 times slower than the rest of the substrate. However, if it is to form an effective uniform membrane surface, autodoping to the lower substrate and to 35 the upper device layer must be prevented or minimized.

This is accomplished in one method by epitaxially growing a SiGe layer of less than 4,000Å ($1\text{\AA} = 10^{-10}\text{m}$) and less than 25% Ge on either side of the barrier etch stop. The SiGe layers and the barrier etch stop layers are subsequently removed after formation of the membrane in order to complete device dielectric isolation.

The MDI process for forming a dielectric membrane requires that the dielectric material be deposited in net surface tensile stress and that the tensile surface stress level be 2 to 100 times less than the fracture strength of the dielectric. Consideration is also given to matching the coefficient of thermal expansion of the semiconductor material and the various dielectric materials being used in order to minimize the extrinsic net surface stress of the membrane. Thermally formed silicon dioxide forms as a strongly compressive film and most deposited dielectrics currently in use form typically with compressive surface stress. High temperature silicon dioxide and silicon nitride dielectric deposited films with tensile surface stress levels 100 times less than their fracture strength have been demonstrated as large area free standing membranes consistent with the requirements of the MDI process.

It is not a requirement of the MDI process that if a semiconductor material is used in the fabrication of a circuit membrane, that the semiconductor material be capable of forming a free standing membrane. The dielectric materials that are optionally used to isolate any semiconductor devices in the circuit membrane can provide the primary structural means of the resulting circuit membrane as implied by the general fabrication methods presented below.

The ability to form large durable temperature tolerant low tensile stress films of both semiconductor and dielectric materials as components or layers of a

substrate for the fabrication of integrated circuits and interconnect structures is unique to the MDI process. The large free standing semiconductor and dielectric membrane substrates of the MDI process provide unique structural advantages to lower the cost and complexity of circuit fabrication and enhance the performance of circuit operation.

The MDI process can be broadly described as two methods, depending on which method of forming the semiconductor substrate thin film is selected. The sequence of steps of the two process methods presented below may be utilized in a different order depending on processing efficiencies. Formation of polysilicon or a-Si (amorphous silicon) circuit devices on a dielectric membrane without the starting use of a semiconductor substrate is disclosed below, but is not categorized as a method.

Method #1

1. Implant, diffuse, or epitaxially grow an etch barrier layer in over the silicon substrate.
2. Optionally grow the desired epitaxial device layers.
3. Optionally trench isolate the semiconductor device areas.
4. Complete all desired IC processing steps including deposition of a low stress dielectric membrane.
5. Form a dielectric and semiconductor substrate membrane by selectively etching the back side of the substrate to a barrier layer or to a controlled substrate residual.
6. Complete the IC processing steps on the back side of the substrate and remaining top side of the substrate, and optionally trench isolate the

semiconductor devices if not done in step 3.

Method #1 fabricates the desired semiconductor devices of an IC on a standard thickness semiconductor substrate 10 prior to the deposition of the low stress dielectric membrane and release of membrane structure 14 by etching the back side of the substrate. (Figure 1a shows in cross-sections the substrate 10 after back side etching.) These semiconductor devices will typically be trench isolated (see below) through or below the active area layer of each semiconductor device.

The semiconductor devices will typically be fabricated from vapor phase epitaxial depositions. Well known epitaxial fabrication methods such as SEG (Selective Epitaxial Growth), ELO (Epitaxial Lateral Overgrowth), MOCVD (Metal-Organic Chemical Vapor Deposition) or MBE (Molecular Beam Epitaxy) may be employed.

In the embodiment of Figure 1a an etch stop barrier layer 12 is implanted just beneath the surface of the silicon substrate 10. This is shown in Figure 1b, which is an expanded view of a portion of substrate 10 prior to the backside etching step. Portion 11 of substrate 10 is to be removed. This barrier etch stop layer 12 may be an oxide layer produced in a manner similar to the well known SIMOX technique or an implanted silicon nitride layer; however, the thickness of the buried oxide or nitrid layer required for MDI processing is significantly less than that required to achieve device dielectric isolation for a silicon substrate which is the general application for such implant technology. (The term SIMOX (Separation by IMplanted OXygen) is a general reference for the dielectric isolation process of forming a buried layer of SiO₂ in a bulk silicon substrate by oxygen implant.) The purpose of layer 12 is to induce minimum damage to the crystalline surface of the substrate 10 which would degrade subsequent semiconductor device processing, while

providing a uniform substrate (silicon) preferential back side etch stop just beneath the surface of the substrate. The barrier etch stop layer 12 can be made at a well controlled thickness and acts as an end point when the 5 silicon substrate 10 is selectively etched from the back side 14 (see Figure 1a) as part of the processing in forming the low stress dielectric and (optionally) semiconductor circuit membrane. The barrier etch stop 12 as shown in Figure 1b does not extend to the edge of the 10 substrate. It is not restricted from extending to the edge of the substrate (wafer), but it must extend beyond that portion 11 of the substrate 10 that will be removed during the formation of the membrane structure.

The original substrate upon which the MDI circuit 15 membrane is formed serves as retaining frame (or ring) 18 for the MDI circuit membrane after the backside of the substrate is etched. The backside etch of the substrate leaves the frame 18 of the substrate to hold the resulting circuit membrane. The width of frame 18 is sufficient to 20 prevent the surface forces of the circuit membrane from causing the frame to crack. A width typically of less than 400 mils (1 cm) is sufficient. This is done by growing thermal oxide and or depositing a film typically of silicon nitride (about 5,000Å to 7,500Å thick) on the 25 backside 14 of the substrate and then etching a window or opening in dielectric layer the size and shape of the desired circuit membrane. The substrate is then etched through dielectric window or dielectric mask. The shape of the backside window opening (or dielectric mask) is 30 typically rectangular, although it can vary in shape.

The barrier etch stop layer 12 is then selectively etched to leave only the original surface 10 layer of the silicon substrate. A barrier etch stop layer could also be formed on the surface of the silicon substrate if the 35 layer preserves sufficient crystalline structure required

for subsequent epitaxial processing, surface stress (typically less than 10^4 dynes/cm² tensile) and there is a selective etch procedure for the silicon substrate versus the barrier etch stop layer, and if need be, the applied 5 barrier etch stop layer can subsequently be removed. Th backside 14 is etched away by TMAH (tetra-methyl ammonia hydroxide) or other appropriate selective silicon etchant (see below). Figure 1c shows formation of the semiconductor devices 24, 26, 28 in the semiconductor 10 substrate after backside substrate etch to a buried etch stop layer, dielectric deposition, and selective removal of the barrier etch stop. Trenches 25, 27, 29 are cut into the substrate 10 prior to deposition of the low stress dielectric membrane 20, which also serves as an 15 isolation dielectric between adjacent semiconductor devices 24, 26, 28.

An alternative technique to trench isolation as suggested by either steps 3 or 6 of Method #1 in order to laterally isolate transistor devices of the circuit 20 membrane is to use the well known LOCOS (LOCAL Oxidation of Silicon) isolation method. LOCOS could be applied as part of the processing of step 6 (process steps 4 or 5 in Method #2 below) as shown in Figures 1d and 1e. Figure 1d shows in cross-section several transistors 11a, 11b, 11c 25 of a circuit membrane 20 with semiconductor layer 20b, interconnect metallization 20c, low stress dielectric membrane 20d, and with completed topside device processing and a backside deposited low stress silicon nitride mask 13 patterned with openings 15a, 15b between transistors. 30 Subsequent thermal oxidation 17a, 17b of the thin silicon device substrate layer underneath the openings in the nitride mask 13, as shown in Figure 1e, laterally isolates the transistors 11a, 11b, 11c and results in complete dielectric isolation of the circuit membrane transistors 35 11a, 11b, 11c.

The thermal oxide isolation created by the LOCOS method may change the net tensile surface stress of the semiconductor (substrate) membrane layer. The deposition of low stress dielectric films on either side of the 5 semiconductor layer prior to LOCOS processing will offset most compressive effects of the oxide formation. Device isolation by the LOCOS process when applied to a MDI circuit membrane is more effective than current bulk processing because of the shallow depth of the 10 semiconductor substrate layer. This also allows near optimum density of the circuit devices with respect to minimum device isolation separation. The easy incorporation of LOCOS into the MDI processing methods also is an indication of the general compatibility of the 15 MDI process with existing IC fabrication techniques.

The remaining substrate 10 (see Figure 1f) is then (optionally) bonded at its edges to a bonding frame or ring 19 (which is typically of glass, quartz or metal and about 25 to 100 mills thick) by conventional anodic, fusion 20(thermal) or epoxy bonding techniques. In this case the substrate frame 18 may be removed (see Figure 1g). The bonding frame or ring 19 is not required for processing MDI; the original substrate 10 (which is backside etched) performs this function initially.

25 An alternative to forming a barrier etch stop layer is to polish the silicon wafer 10 on both sides to a thickness uniformity specification such that when the substrate is selectively time etched from the back side, the etch can be stopped prior to reaching the dielectric 30 membrane 20 and will leave an acceptably uniform thickness for the active device substrate. This method is mechanically difficult in that it requires the wafer to be exactingly polished on both sides to achieve the uniform thickness.

35 The dielectric membrane 20, 36 is formed as part of

the interconnect metallization dielectric and as a layer over the two-sided interconnect metallization 35 as shown in Figures 3a and 3b. (Figure 3b is an enlarged view of the portion of Figure 3a referenced as "3b".) The thickness of the dielectric membrane 20, 36 may vary from less than 2 μm to over 15 μm per layer of interconnect metallization layer 35. All blanket dielectric material covering the substrate has a low stress surface tension and is preferably in tensile stress.

10 Two sided interconnect metallization 35, with low stress dielectric material 36 (see Figure 3b) used as the interconnect dielectric can be applied, or the back side of the circuit membrane can be passivated with low stress dielectric for a conventional one-side interconnect structure. The circuit membrane can withstand processing temperatures in excess of 400°C. which is required for further deposition of various low stress dielectric layers such as SiO_2 and Si_3N_4 , and to achieve reliable low resistance junctions between semiconductor device 20 electrode contacts and interconnect metallization. Depending on the specified composition and thickness of the dielectric and substrate membrane material, higher temperature processing steps can be performed such as may be required by implant activation annealing or epitaxial 25 processing.

The alignment of lithography tools on the back side of the substrate is performed through the transparent dielectric material as shown in Figure 4. The semiconductor substrate material 10a near the alignment 30 mark 40 (which is nearly transparent in the visible portion of the spectrum at thicknesses less than 2 μm) can be etched away from the dielectric membrane 20 so that the lithography alignment marks 40 are more readily visible. Infrared alignment mechanisms are also available for back 35 side alignment; silicon is transparent at infrared

wavelengths. Lithography marks 40 for infrared alignment cannot be as small as those used in the visible spectrum due to the longer wavelengths of the infrared, typically greater than 6,000Å.

5 Method #2

1. Form a free standing low stress semiconductor substrate membrane.
2. Optionally grow the desired epitaxial device layers.
- 10 3. Complete all desired top side IC processing steps including deposition of a low stress dielectric membrane.
4. Optionally trench isolate the semiconductor device areas from the back side.
- 15 5. Complete IC processing steps on the back side of substrate and remaining top side of substrate.

IC processing steps used on the top side and backside of the semiconductor membrane substrate are well known and not unique in application to the semiconductor substrate 20 membrane; nearly any semiconductor process technique can be applied.

Method #2 fabricates a thin low stress semiconductor substrate membrane 20, such as the one shown in Figure 2, prior to deposition of the low stress dielectric membrane 25 and fabrication of semiconductor devices. This substrat membrane as shown in Figure 2 can be formed through established selective electro-chemical etching techniques or by combination of wafer bonding, grinding and selectiv substrate etching techniques. The membrane preferably has 30 a tensile stress of approximately 10^8 dynes/cm². (This can be achieved in one manner by forming a layer with n-type dopant concentrations of 10^{16} to 10^{19} atoms/cm² and applying electrochemical etch techniques.) After the semiconductor substrate membrane 20 is fabricated (see Figure 3a),

semiconductor devices 24, 26, 28, ..., 30 are fabricated and interconnected on the substrate 20 with the use of 10 stress dielectric material. The low stress dielectric membrane formed on the semiconductor substrate (along with 5 interconnect metallization) becomes the only structural circuit membrane component after the semiconductor substrate portion of the membrane is etched or trenched into independent semiconductor devices. An additional layer (not shown) of low stress dielectric over the 10 interconnect metallization may be applied for passivation and to increase the thickness of the resulting membrane 20 to achieve a specific desired level of durability.

The back side etch of the semiconductor substrate 14 (see Figure 2) permits the under side of the semiconductor 15 devices 24, ..., 30 to be accessed and additional processing of the semiconductor devices performed. The processing options on the under side of the semiconductor devices 24, ..., 30 are the same as those for Method #1; however, trench isolation (see Figure 1c) of the 20 semiconductor devices has not as yet been performed. Trench isolation is the etching of a separation space 25, 27, 29 (typically less than 2 μm wide) between semiconductor devices 24, 26, 28 on all sides of the 25 semiconductor devices and is an established IC process technique. The space or trench 25, 27, 29 is then filled with dielectric. Trench isolation is novel as applied here, because the technique is being applied to a semiconductor membrane supported by a dielectric membrane. If trench isolation is desired, established masking and 30 etching techniques can be applied to form trenches.

The uniformity of the semiconductor substrate thickness is important to the uniformity of the operating characteristics of the semiconductor devices of an IC, and to lithography processing steps. The above-described 35 embodiments use etch stop techniques when selectively

etching the semiconductor substrate material to form the desired substrate membrane thickness.

The interconnect circuit membrane can also be formed on a glass or quartz substrate 23 (typically less than 50 5 mils thick). In this case a tensile film 25 of polysilicon (as taught by L.E. Trimble and G.E. Celler in "Evaluation of polycrystalline silicon membranes on fused silica" J. Vac. Sci. Technology B7(6), Nov/Dec 1989) is deposited on both sides of the substrate 23, as shown in 10 Figure 1h. A MDI interconnect circuit membrane 27 is then formed on the polysilicon membrane 25, as shown in Figure 1i. An opening 29 in the polysilicon 25 on the backside of the substrate 23 is made and the back of the substrate 23 is selectively etched leaving a free standing tensile 15 polysilicon membrane 27 held in the frame 23b of the remaining substrate, as shown in Figure 1j. The polysilicon 25 directly beneath the circuit membrane 27 can optionally be removed as also shown in Figure 1j. A metal film (not shown) or other protective layer is 20 deposited over the circuit membrane prior to etching the backside of the substrate to protect the circuit membrane from the substrate etchant. Considerations for using a non-semiconductor substrate in the fabrication of MDI 25 interconnect circuit membrane are substrate material cost or application requirements. Examples of applications for this approach to membrane fabrication are masks for high resolution conformal contact lithographic printing and MCM (Multi-Chip Module) interconnect circuits.

Low Stress Silicon Dioxide and 30 Silicon Nitride Deposition Recipes

Low stress dielectric membranes have been manufactured consistent with MDI requirements for low stress high temperature dielectric films. These membranes were produced on Novellus Systems, Inc. (San Jose, CA)

Concept One dielectric deposition equipment, but are not limited to such equipment. Low stress is defined relative to the silicon dioxide and silicon nitride deposition made with the Novellus equipment as being less than 8×10^8 5 dynes/cm² (preferably 1×10^7 dynes/cm²) in tension. Acceptable surface stress levels of different dielectrics made on various equipment may vary widely.

The following are two typical recipes used to produce the dielectric membranes of silicon dioxide or silicon 10 nitride required by the MDI process. Variations of these recipes can be used to emphasize specific characteristics of the deposited dielectric membrane; these recipes are not the only recipes to achieve the requirements of the MDI process on the Novellus equipment and are not 15 limitations on the MDI process. Small variations in the parameters of the recipes can produce changes in the material structure, etch rate, refractive index, surface stress, or other characteristics of the deposited dielectric material.

	<u>Recipe #1</u>	<u>Recipe #2</u>
	Silicon Dioxide	Silicon Nitride
Temperature	400°C	400°C
Pressure	1.8 Torr	2.3 Torr
HF RF Power	640 watts	220 watts
25 LF RF Power, 100 ohms	160 watts	180 watts
SiH ₄	260 sccm	0.23 slm
NH ₃	--	2.00 slm
N ₂	1150 sccm	0.60 slm
30 N ₂ O	6000 sccm	--

Structurally Enhanced Low Stress
Dielectric Circuit Membranes

Figure 5 shows a structurally enhanced MDI circuit membran structure. Structural enhancement of the MDI

circuit membrane may prove necessary for various applications where stress is applied to the membrane as part of normal operation, such as in pressure sensing or in making contact test measurements as in IC wafer sort testing. A portion 44 of the dielectric membrane is deposited over the SD layer 24a with a thickness greater than 1 μm , and typically 10 to 25 μm . This thicker deposited layer 44 of the dielectric membrane is patterned with a mask and dry etched to achieve a honeycomb-like pattern of recesses 46a, 46b, 46c. The depth of these recesses 46a, 46b, 46c is approximately 75% of the thickness of the low stress dielectric 44 in which they are etched. Optional electrical contact 47 is provided and shown as an example of a circuit electrode. The dimensions of the opening of the recesses 46a, 46b, 46c are typically two or three times the depth dimension. A deposition of 1,000 \AA of low stress CVD silicon nitride may optionally be applied to form a passivating seal.

MDI Air Tunnel Interconnect Structure

The impedance of metal conductors (traces) that make up the interconnect metallization between semiconductor devices and passive circuit elements such as capacitors or resistors must be given careful design consideration at operational frequencies in excess of 100 MHz. The dielectric constant of a dielectric (insulating) material is a primary determining factor when consideration is given to the use of the material. Polyimide materials conventionally used in the construction of interconnect structures have dielectric constants typically ranging between 2 and 3.5. The dielectric constants of CVD silicon dioxide and silicon nitride typically range upward from 3.5. The ideal dielectric is vacuum, gaseous or air with a dielectric constant of approximately unity. The fabrication of an interconnect structure that isolates the

majority of a conductor's surface area with vacuum or gaseous dielectric results in a near optimum condition for high speed operation of that structure. Trac or conductor structures called "Air Bridges" are fabricated 5 on the surface of an IC contacting the surface of the IC only periodically. This periodic contact provides mechanical support and or electrical contact with a low net dielectric constant of isolation. Air Bridges are conventionally used in the fabrication of microwave 10 circuits; such circuits have operational frequencies in the GHz range.

Figures 6a, 6b and 6c show cross-sectional views of a conductor structure 50 internal to dielectric layer 52, 52a, but which has a gaseous primary surface dielectric 15 contact with only periodic mechanical contact 50-a, 50-b, 50-c, like the conventional Air Bridge. The conductor 50 is held suspended in the gaseous dielectric without contacting the surrounding or enclosing solid material structures. Figure 6d is a top view of a portion of a 20 conductor or trace showing column supports (and/or via contacts) 50-a, 50-b, 50-c and dielectric support columns 52-a, 52-b. This interconnect structure is herein called an "Air Tunnel", and its method of fabrication is a direct extension of the methods used in the above-described 25 fabrication of the MDI circuit membranes (dielectric and semiconductor membranes). Also shown in Figures 6a, 6b and 6c are dielectric membrane 56, semiconductor membrane 58, dielectric support column 52a, ground plane metallization 60, cavity 54 formed by etch removal of a-Si 30 (amorphous silicon), and opening 62 for etch removal of all the a-Si. Figure 6b is an end-on view of an alternate structure to Figure 6a. Figure 6b shows dielectric plug contact 68 to support (suspend) conductor 50. Figure 6c shows an extension of the structure of Figure 6a with a 35 second layer of dielectric 70 and traces 72.

The Air Tunnel structure can be fabricated on any semiconductor substrate in addition to an MDI circuit membrane. The structural dielectric materials used are selected from the same group of low stress dielectrics used in the fabrication of the MDI circuit membranes discussed above. The fabrication method for the Air Tunnel provided here can also be extended to the gaseous dielectric isolation of semiconductor devices and passive circuit elements in a circuit membrane.

- 10 The Air Tunnel structure in one embodiment is fabricated with CVD processing techniques; alternatively, ECR (Electron-Cyclotron-Resonance) plasma CVD processing may soon provide an alternative deposition method. The gaseous dielectric separation of a conductor or a 15 semiconductor device is accomplished by forming a sacrificial CVD film of a-Si, polysilicon or alternate material (typically dielectric material) that can be deposited by CVD means and selectively etched versus the other MDI circuit membrane material layers. Anticipating 20 the use of Air Tunnel interconnect structures in the fabrication of a circuit membrane, semiconductor devices are isolated (passivated) by trench isolation of each device, and depositing a thin layer of oxide or nitride (typically less than 2,000Å thick) over exposed device 25 surfaces, and then depositing a film of a-Si. The thickness of the a-Si film and the width of the isolation trench are chosen such that the trench is plugged or filled evenly leaving the surface over the plug relatively planar. This plug technique is facilitated by CVD process 30 technology which deposits films conformally on all interacting surfaces. Subsequent Air Tunnel interconnect structures are completed and the a-Si layers are removed by a silicon selective etchant; the etchant accesses the a-Si through the etch-vias as explained below.
- 35 The fabrication method of Air Tunnel interconnection

is independent of the underlying substrate. The underlying substrate could be a MDI circuit membrane as shown in Figure 6d (fabrication of which is disclosed above), a conventional IC substrate of semiconductor devices, a MCM circuit substrate, MDI tester surface membrane, etc.

The Air Tunnel fabrication process begins (see Figure 6f) with the deposition of an a-Si film 76 onto a substrate 56 with electrodes to be interconnected. The a-Si film 76 is patterned with trenches and contact vias. A CVD processed metal film 50, typically tungsten (W), is deposited over the a-Si. The dimensions of the a-Si trenches and vias in the a-Si layer are consistent with forming planar plugs. The trenches in the a-Si 76, once plugged with the metal film 50, become the support columns 50-a, 50-b, 50-c of the conductor, see Figures 6a and 6d. The conductors deposited in the vias provide mechanical (column) support and electrical contact. The metal film 50 is patterned and a second CVD processed a-Si film 78 deposited over the metal film 50; a thin layer (not shown in Figure 6a) of highly conductive metal like Au or Cu may be sputter deposited over the CVD metal (prior to the patterning of the metal film 50) to enhance conductivity of the conductor. The a-Si film 78 is patterned as shown in Figure 6f, removing the a-Si film 78 from over the metal conductor 50 and forming a trench 80 along the edge of the conductor 50. This trench is plugged by a 3rd CVD layer 82 of a-Si, as shown in Figure 6g. The patterning of the second a-Si layer 78 over the metal conductor 50 does not require a critical alignment; an alignment tolerance of +50% of the thickness of the second a-Si layer 78 is sufficient.

The resulting three films 76, 78, 82 of a-Si are relatively planar with minor surface features along the edges where conductors 50 are directly beneath. These

surface features can be reduced by shallow thermal oxidation of the a-Si surface and subsequent stripping of the oxide (not shown).

An alternative method that can be used to planarize the a-Si and metal films is to spin coat a thick polymer over substrate 75, low stress dielectric 77, first a-Si layer 79, and second a-Si layer 81 after the application of the second a-Si film 81. (This a-Si film 81 is deposited in thickness equal to the combination of the former second and third a-Si films.) The polymer 85 used is selected to have a RIE rate nearly identical to the that of the a-Si film. The polymer 85 is completely removed and the etch of the a-Si is continued as desired, see Figures 6h and 6i.

15. The a-Si film stack is then patterned to form trenches that will become the supporting columns 50-a, 50-b, 50-c of an over layer of low stress dielectric. These support columns are typically placed in a non-continuous manner along conductors 50 (as shown in Figure 20 6d), and periodically placed across open areas 51 where there are not conductors. The periodic and overlapping placement of the support columns (etch-vias) increase the ability of a-Si selective etchant to remove all deposited a-Si material. The thin metal film 60 (see Figure 6a) of 25 typically less than 5,000Å thickness may optionally be deposited over the patterned a-Si prior to the deposition of the low stress dielectric film to act as a ground plane and EM (Electro-Magnetic) shield for the conductor 50. (This metal film remains in contact with the overlying low 30 stress dielectric film after the a-Si has been removed.) A low stress dielectric film 52, 52a is deposited of typically 1-2 µm thickness over the patterned a-Si films. This low stress dielectric layer 52, 52a is patterned with trench openings 62 to the a-Si films. These trench 35 openings are called etch-vias and provide access for a

a-Si selective etchant like TMAH or ethylene diamine to remove all of the internal layers of a-Si films from each layer of interconnect without regard to the number of layers.

5 The etch-vias 62 in the dielectric are placed near dielectric support columns as shown in Figures 6c and 6d. The etch-vias 62 are placed on every interconnect layer and with sufficient frequency per layer to allow etchant to reach all lower layers of the Air Tunnel interconnect 10 structure. After the etch-vias 62 are formed an additional interconnect layer 72, 80 (see Figure 6c) can be formed by repeating the sequence of process steps as outlined below. When the Air Tunnel interconnect structure is used on a semiconductor membrane to form a 15 circuit membrane (MDI process), it should be clear that the application of the Air Tunnel to both sides of the semiconductor membrane is a natural extension and not a special case application requiring a different processing sequence.

20 The etch-vias 62 serve as access ports for gaseous material (such as N₂ or air) which allow the effective circuit dielectrics to enter the circuit membrane. The etch-vias 62 also serve to maintain equalized pressure between the internal interconnect structure and the 25 external environment of the surface of the circuit.

The following sequence of processing steps for fabricating an Air Tunnel assumes that the substrate being processed has an existing layer of low stress dielectric film on which to start:

- 30 1. Pattern dielectric for metal contact plug vias and etch-vias.
2. Deposit a film of a-Si; the thickness of this film will determine the lower separation distance of the tunnel conductor from the underlying low stress dielectric.

35

3. Pattern a-Si film for conductor support columns
(vias to underlying dielectric).
 4. Deposit metal conductor film.
 - 5a. Pattern metal conductor film.
 - 5b. Optionally deposit high conductivity metal film before patterning conductive film.
 - 6a. Deposit a-Si film approximately the thickness of the metal film.
 - 7a. Pattern a-Si film to expose conductor surfaces and trench etch along sides conductors.
 - 8a. Deposit a-Si film to planarize the surface and separate the conductor from the overlying dielectric film.
 9. Pattern a-Si film for dielectric support columns
(vias to dielectric).
 10. Optionally deposit ground/shield metal film.
 11. Deposit low stress dielectric film.
 12. Pattern dielectric with etch-vias or repeat from first step above.
- 20 Steps 6 through 8 from above can be replaced with the following alternative steps for forming a planarized conductor layer:
- 6b. Deposit a-Si film with a thickness equal to the thickness of the conductor and the desired separation over 25 the conductor.
 - 7b. Deposit planarizing polymer with a etch rate that is very similar to that of the a-Si film, as shown by Figure 6h.
 - 8b. RIE until all polymer material has been removed, 30 as shown by Figure 6i.
- The principle attributes of the Air Tunnel are:
1. Low average dielectric constant (approaching unity).
 2. Self planarization fabrication method.
 - 35 3. Integral ground or EM shielding plane.

4. Application to one or both sides of a circuit membrane.
 5. Application to MDI circuit membranes or standard wafer substrates.
- 5 A MOSFET device connected by Air Tunnels is shown in cross-section as an example in Figure 6e. The transistor of Figure 6e is formed from a semiconductor membrane and held suspended by the metal contacts to its electrodes with a gaseous dielectric separation on all remaining 10 device surfaces. Shown in Figure 6e are the active portion 84 (MOSFET) and the unused portion 86 of the semiconductor membrane, a thin nitride isolation film 88, mechanical conductor support 94, conductor trace 92, and additional air tunnel interconnect structures 92, 94, 96.

15 MDI Circuit Membrane Advantages

The fabrication of circuit membranes provides the capability to fabricate and use integrated circuits in novel ways such as:

1. Back side interconnect metallization, backside 20 SD electrode contact, and through-the-dielectric membrane interconnect metallization signal routing. (See Figure 3b).
2. The use of optical communication (see Figure 7) in a vertically arrayed stack of MDI circuit membranes 25 150a, 150b, 150c with optical transmit and receive semiconductor devices on either side of the circuit membranes. Busing of data through a stack of several MDI circuit membranes 150a, 150b, 150c from any point on the surface of an IC rather than forming connections at the 30 edge of ICs (which is currently the practice) simplifies the structure of the circuit. An external communication optical transceiver 152 is provided. MDI circuit membrane 150b includes a transparent window 154 through which optical transmissions from transmitters (laser diod

arrays) 156 pass to optical receiver SDs 158. The stack of MDI circuit membranes is held together by support 160. The ability to use optical means rather than metal conductors to transmit information between ICs shortens the length of the communication path, increases the speed and bandwidth of the communication path, and lowers the power consumed compared to present metal connection methods.

The optical receiver of the MDI circuit membrane is typically less than 5,000Å in thickness. A receiver of this thickness will absorb only a portion of the optical signal fluence striking it, the remainder of the fluence will pass through and out the opposite side of the receiver. This permits a second or third receiver to be positioned in the path of the optical transmitter to receive the same signal. The limiting conditions that determine the number of receivers that can be associated with one transmitter are the output fluence of the optical transmitter and the thickness of the transceiver substrate. This ability to optically transmit to several receivers simultaneously has the benefits of reducing circuit complexity (versus a transceiver structure at every circuit membrane interface) and performance (no transceiver (repeater) propagation delay).

3. The vertical bonding of two or more circuit membranes to form a three dimensional circuit structure, as shown in Figure 8. Interconnection between the circuit membranes 160a, 160b, 160c including SDs 162, 164, 166 is by compression bonding of circuit membrane surface electrodes 168a, 168b, 168c, 168d (pads). Bonding between MDI circuit membranes is achieved by aligning bond pads 168c, 168d (typically between 4 µm and 25 µm in diameter) on the surface of two MDI circuit membranes 160b, 160c and using a mechanical or gas pressure source to press the bond pads 168c, 168d together. If the pads

168c, 168d are solder, they can be heated to the melting point of the solder (typically less than 350°C) causing the pads to weld to each other. If the pads are indium, tin, or alloys of such metals, a bond 170 will form 5 between the metal pads 168c, 168d with the application of approximately 100 p.s.i. pressure and an application temperature between 50°C and 400°C, depending on the metal or alloy selected.

4. MDI Nanometer width gate MOSFET device
10 fabrication methods. The ability to fabricate a MOSFET device with a gate region length of less than 0.5 μm (500 nm) presently requires lithograph tools with greater resolution capability than the current high volume optical stepper tools. Several methods are presented here for the 15 fabrication of MOSFET with gate lengths of less than 500 nm ^{19C} and capable of gate lengths less than 25 nm. These methods take advantage of the MDI process to form transistor gate regions of less than 500 nm (.5 μm) without lithographic means are described hereinafter.

20 5. Sensor diaphragms formed with integrated circuits fabricated on conventional rigid substrates.

6. Fabrication of electrically isolated semiconductor devices on both sides of the semiconductor layer of a circuit membrane.

25 V-Groove Transistor Region Gate Formation Method

Figures 9a to 9e show a sequence of steps for forming a p-channel or n-channel (npn) transistor with an opposed gate electrode and a gate width of less than 25 nm (250Å). The process steps (see Figure 9a) assume a starting 30 substrate of an MDI circuit membrane with approximately 0.5 to 1.5 μm wide isolated metal gate electrode 174 fabricated on the backside (opposed) of the transistor. This MDI circuit membrane consists of a lightly doped <100> crystalline silicon membrane layer 176 of thickness

typically less than 2 μm and a 1 to 2 μm layer of low stress dielectric 178.

The sequence of process steps for one embodiment is:

1. Form lightly doped p and n wells. Figure 5 shows one such well 180. This is done by depositing a nitride layer 182 over the silicon layer 176 of the MDI circuit membrane, patterning the well 180 and implanting the desired dopant.
2. Deposit dielectric 184 (see Figure 9c) and pattern an opening 0.75 to 1.25 μm wide over the opposed gate area, but a known width. 10
3. Anisotropically etch along the <111> crystalline planes of the silicon to form a V-groove 186 of known depth and side angle of 54.7 degrees. 15 This is done with a time rated etch.
4. Deposit by CVD equipment a metal layer 190 such as tungsten of 0.5 to 1.5 μm , but of known thickness, just closing the V-groove 186.
5. Etch back the metal layer 190 until a known thickness of metal plug remains in the V-groove 186. The width of the resulting transistor gate length is determined by the dimension of the remaining metal in the V-groove. 20
6. Strip the dielectric mask 184 in Figure 9c.
7. Etch the silicon 180 surface to just expose the metal plug 190 opposed to the gate 174. 25
8. Deposit a dielectric layer and pattern for heavy implant doping 192 of transistor source and drain regions. This is done with n and p doping separately leaving a lightly doped gate channel region 194. 30
9. Strip the dielectric mask in Figure 9e and etch the silicon 180 surface until it is below the level of the metal plug 190, causing its removal. 35 (This step is optional, the metal plug can be

selectively etch removed.)

10. Form trench 196 to isolate transistors to under the layer of low stress dielectric 178.

11. Anneal the active transistor implants 192.

5

12. Form source and drain contacts 198.

13. Anneal the source and drain contacts 198.

It should be clear that the opposed gate electrode which is much wider than the actual length of the gate width could have been fabricated on top of the transistor 10 with the source and drain contacts, or after the gate region of the transistor was formed.

The reliable fabrication of the gate region 194 at a known length is dependent on etch rate control. Present etch rate techniques support the capability to form a gate 15 region 194 length of less than 25 nm. A CVD dielectric could also be used as the gate implant mask instead of a metal plug 90. This gate fabrication method can also be done in bulk silicon and is not limited to the MDI process. It is important to note that the sub-micron 20 resolution of the gate region was achieved without lithographic means capable of sub-micron resolution.

Figures 9f, g, h, i & j show the process sequence for substrate-imaged nonlithographic MOS transistor gate region or Bipolar emitter region formation. This process 25 takes advantage of the novel ability of the MDI structure to accommodate process steps on either side of the membrane substrate. This process can form a minimum feature size of less than 100 nm and does so by the use of anisotropic etching epitaxial processes.

30 Figure 9f shows a MDI substrate of semiconductor 189 and low stress dielectric 191 formed by one of the methods presented above. The dielectric layer 191 on one side has been patterned and the semiconductor layer 189 anisotropically etched through to the dielectric layer 193 35 on the opposite side. The thickness of the semiconductor

layer 189 is selected to be less than 2 μm , and the dielectric layers 191, 193 are less than 1 μm thick each, though these dimensions can be scaled to achieve any transistor dimensions. The size of the patterned opening 5 195 in the dielectric is chosen such that the etched opening 197 onto the underlying surface of the dielectric is a desired width, less than 100 nm. Widths of any dimension can be created, however, widths of less than 100 nm are the primary objective of this process which 10 cannot be achieved by optical means. The patterned dielectric 191 has a 1,000-2,000 \AA layer 199 of low stress silicon nitride to provide high selectivity versus the opposed dielectric layer during a subsequent RIE process step.

15 Figure 9g shows an opening 197 formed through the dielectric layer 193 opposite the patterned layer 191. The anisotropically etched semiconductor layer 189 with its opening 197 onto the under side of the opposite side dielectric was used as a substrate-imaging mask, and the 20 dielectric layer 193 was etched by RIE (dry) processing. This substrate-imaged opening 197 can be less than 100 nm in diameter and will become the gate region of a MOS transistor or the emitter region of a bipolar transistor. Figure 9h shows the substrate-imaged region 197 closed by 25 selective epitaxial growth 201; the epitaxial growth 201 can be formed with a graded dopant structure to lessen short channel effects. Figure 9i shows the formation of a gate oxide 203 and electrode 205 after a planarization step of the self-imaged opening 197, CVD or thermal formed 30 gate oxide and formation of gate electrode. It is important to note that the dielectric layer 193 in which the gate electrode 205 is formed is self-aligned to the gate region.

Figure 9j shows the finished MOS transistor. The 35 side opposite the gate electrode 205 is stripped of

dielectric, planarized and etched to a thickness of less than 2,500Å. It was then trenched 207 for source/drain isolation, a layer of low stress dielectric 209 deposited and source/drain electrodes 211, 213 formed.

5 It should be clear to some skilled in the art that a bipolar transistor can be formed with somewhat similar fabrication steps.

MDI Lateral Epitaxial Grown
Transistor Gate Region Fabrication

10 Figures 10a, b, c, & d show a method for forming a MOSFET transistor with transistor gate region lengths of sub-micron dimensions, without the requirement for lithography tools with sub-micron CD resolution capability. This method is an extension of the above-
15 described MDI process technology.

In Figure 10a, the starting substrate structure is a combination silicon and dielectric 204 film forming a membrane 202. This membrane 202 is formed by one of the methods disclosed above. Subsequently, membrane 202 is
20 patterned for the doping of the n+ and p+ transistor channels. Figure 10a shows a cross-section of a MOS transistor channel (source 210, gate 208 and drain 206 regions) with a nitride mask 212 through which an anisotropically formed gate 208 trench is etched to the
25 underlying dielectric membrane 204 in the location where the gate region of the transistor will be constructed. The exposed silicon sidewall 214 may be polished by a thin thermal oxidation and etch stripping or chemical techniques. Figure 10b shows a top view of the structure
30 of Figure 10a, with the transistor channel 210, 208, 206 isolated from surrounding transistor devices by dielectrically filled trenches 216. These trenches 216 are fabricated prior to etching the gate region trench 208. The gate region trench 208 is then filled (see

Figure 10c) from both silicon sidewalls by lateral selective epitaxial growth of silicon 220 and with the same or similar doping concentration as the adjacent regions 210, 206; source and drain implant doping can also 5 be used as a doping means prior to epitaxially growing the gate region. (In the case of CMOS devices, the n+ and p+ transistor channels are processed in two separate sequences of processing steps.)

The epitaxial growth process in the gate region 10 trench 208 is stopped when the remaining separation distance "d" between the approaching silicon sidewalls 220 is equal to the desired gate region length. The doping concentration is changed for forming the actual gate region 222, and the epitaxial growth is continued until 15 the gate region trench is closed, as shown in Figures 10c and 10d.

The width of the initial gate region trench 208 and the epitaxial growth rate can be controlled with an error of less than 5 nm. This allows the length d of the gate 20 region to be determined by the precision with which the gate region trench 208 can be formed, the deposition rate control of the lateral epitaxial growth 220 and the capability to create the desired doping transitions. The result of this approach means that a gate region length d 25 of 25 nm or less can be formed. This is far beyond the current optical lithographic methods which are presently expected to reach production capability of 120 nm by the end of the decade.

Figure 10d shows the completion of the transistor 30 with source and drain electrodes 226, 224, and an opposed gate electrode 230. The surface of the epitaxially grown gate region 222 is not smooth, but the backside of the gate region 222 is smooth, due to its formation against the underlying low stress dielectric membrane 204. The 35 gate electrode 230 is more easily and reliably formed by

patterning the underlying dielectric membrane 204 from its backside, thereby forming the opposed gate electrode 230. The backside of the gate region 222 is etched free of dielectric with an opening significantly larger than the 5 length d of the epitaxially grown gate region 222; portions of the source 210 and drain 206 regions are also exposed with the gate region due to lithographic tool limitations. Gate oxide isolation 232 is thermally grown or deposited to the required thickness, and a metal or 10 silicide electrode is formed 230.

The overlap of the gate electrode 230 over the source 210 and drain 206 regions of the transistor channel results undesirably in performance limiting capacitance. The reduction of the capacitance from the overlapping gate 15 electrode structure can be achieved by either epitaxial graded doping of the source and drain regions at the interface to the gate region growth over the gate region, to form an extended gate region, or by offset of the gate electrode so that the source side edge of the electrode 20 aligns approximately with the source/gate interface of the transistor channel. These methods are disclosed below. The above-described MOSFET transistor structure can be converted to a bipolar transistor structure as shown in Figure 12g, also described below.

25 The MDI circuit membrane structure provides the capability to position electrode contacts of semiconductor devices at their backside (or opposed side). This provides significant savings in reduced processing steps to achieve device isolation and new transistor structures.

30 Figure 11a shows a MDI circuit membrane (dielectric 240 and semiconductor 242 films) in cross-section on which additional semiconductor layers were formed epitaxially to achieve either an npn or pnp transistor structure 244. The epitaxial layer 244-a that corresponds to the gate 35 region can be formed with a thickness of less than 25 nm.

Figure 11b shows the dielectric 240 and semiconductor 247, 244, 245 membrane after subsequent well known semiconductor processing steps which form a transistor channel 244 isolated on the dielectric membrane 240 with 5 source 246, drain 248 and gate electrodes 250-a, 250-b attached. Also shown are source region 245 and drain region 247. The gate oxide isolation 251 is thermally grown or deposited, and gate contacts 250-a, 250-b can be formed on one or all sides of the transistor channel. 10 Alternatively, a separate contact 250-b can be formed opposite the gate electrode 250-a, and used as a transistor bias contact. The opposed drain contact 248 is formed by etching a via in the dielectric membrane 240 underlying the transistor drain region 247.

15 Figure 11c shows a bipolar transistor formed by a well known method but on a low stress dielectric membrane 254, and without the requirement to form a lateral conductive path (typically referred to as a buried layer). Formed in semiconductor film 256 are emitter 258, base 20 260, and collector 262 regions. The collector contact 264 is instead formed directly under the emitter 258. It should also be apparent that there are non-silicon semiconductor transistor structures that can be restructured with a backside contact as depicted in 25 Figure 11c, such as a GaAs Heterojunction Bipolar Transistor (HBT) or Ballistic Transistor.

The extension of the gate electrode 250-a beyond the gate region in the fabrication of the MOSFET transistor structure of Figure 11b increases the parasitic 30 capacitance of the transistor, and therefore, adversely affect its performance. This capacitance can be reduced by the separate or combined use of several methods referred to as Graded Gate Doping (GGD), Epitaxially Extended Gate (EEG) and Gate Electrode Offset (GEO).

35 The Graded Gate Doping is shown in Figure 11b. This

method varies the doping levels of the source 245 and drain regions 247 at their respective interfaces to the gate region. This directly decreases the effective dielectric constant of the semiconductor under the dielectric isolation 251 separating the gate electrode from the source 245 and drain 247 regions it overlaps.

The Epitaxially Extended Gate 244-b (see Figure 11d) is formed by selective epitaxial growth of the gate region 244-b over the surface of the transistor upon which the gate oxide 251 and gate electrode 250-a will be fabricated. This method, more directly than the GGD method of Figure 11b, lowers the capacitance of the semiconductor region directly under the gate electrode 250-a where it overlaps the source 245 and drain 247 regions. The transistor capacitive charging effect contributed by the gate electrode 250-a from source 245 and drain region 247 overlap is decreased by these methods, because of the dopant type and dopant concentration relative to the polarity of the applied potential on the gate electrode 250-a. The thickness of the epitaxial layer of the EEG method is determined based upon the desired operating characteristics of the transistor, but typically is less than the dimension of the gate region length.

The extended gate region 244-b of Figure 11d formed by the Epitaxial Extended Gate method can also be a graded doping region. If the extended gate region 244-b is graded, the dopant concentration decreases going away from the gate region (or towards the gate electrode 250-a).

The Gate Electrode Offset (GEO) structure is shown in Figure 11f. Shown are source region 269, gate region 271, drain region 273, semiconductor layer 275, low stress dielectric layer 277, gate oxide 279, and offset gate electrode 281. The drain side edge of the gate electrode 281 is aligned to the drain/gate 273-271 interface of the

transistor channel. The alignment could alternately be made to the source/gate 269-271 interface, and would be a preferred structure under certain device design requirements. The accuracy of the placement of the 5 electrode 281 edge is limited by the capability of the lithography tool used. A gap between the drain region 273 and gate electrode 281 may result leaving a portion of the gate region 271 not covered by the gate electrode 281 due to lithography alignment deficiencies. This can be 10 corrected by extending the drain region 273 through implant doping of the exposed gate region. The size of this gap during manufacturing can reliably be expected to be no greater than the magnitude of the alignment registration error of the lithography tool being used.

15 The transistor structure of Figure 11e used as a bipolar transistor is of interest in order to achieve well controlled fabrication of thin base regions. The contact 270 to the base region 272 of a bipolar transistor in Figure 11e is achieved by epitaxially extending 272-a the 20 base region. This method like the EEG method is the selective epitaxial growth of an exposed region of the transistor that includes the base region 272. Other elements of Figure 11e are collector region 274, collector contact 275, dielectric membrane 276, emitter region 277, 25 and emitter contact 278.

MDI Transistor Fabrication Based on Confined Laterally Doped Epitaxy

Selective growth of high quality epitaxial films in a confined volume was reported in a paper ("Confined Lateral 30 Selective Epitaxial Growth of Silicon for Device Fabrication," Peter J. Schubert, Gerold W. Neudeck, IEEE Electron Device Letters, Vol. 11, No. 5, May 1990, pag 181-183). This "CLSEG" (Confined Lateral Selective Epitaxial Growth) method was developed to achieve

dielectric isolation of crystalline silicon.

Figures 12a, b and c show the use of a MDI circuit membrane to produce a confinement cavity for the epitaxial growth of crystalline silicon. The original objective of 5 CLSEG, to fabricate a dielectric isolated semiconductor substrate, is not an objective here because the MDI process is itself a dielectric isolation process. What is taught here is the application of the capability for growing epitaxial films in a confinement cavity within the 10 context of the MDI process, and a processing method for using confined lateral epitaxial growth to fabricate MOSFET transistors with arbitrarily narrow gate region lengths without the use of lithographic means.

MDI confined lateral doped epitaxial closely controls 15 transistor geometry in all three dimensions: height (as deposited semiconductor film thickness), width (placement of isolation trenches) and source, gate, drain regions (epitaxial deposition thickness). This makes the device operational characteristics more predictable with lower 20 manufacturing complexity. *AF/C*

The MDI Confined Lateral Epitaxy method begins with a membrane of two films, one film 280 of semiconductor (silicon) and one film 282 of low stress dielectric. This membrane 280, 282 is made by one of the methods disclosed 25 above. Dielectric filled isolation trenches 284 (see Figure 12b, a top view of the structure of Figure 12a) are fabricated to form what will become the sides of the transistor channel in the semiconductor film. Then a low stress dielectric layer 290 typically of 1 μm or less 30 thickness is deposited, and a window 286 is anisotropically etched through the semiconductor film 280 stopping on the dielectric layer 282 and positioned between the isolation trenches 284, as shown in Figures 12a and 12b. In the preferred embodiment the orientation 35 of the window 286 is approximately aligned with the

crystallographic orientation of the semiconductor film 280 in order to produce a seed crystal walls 292-a, 292-b of Figure 12c that is at a right angle to the isolation trench walls 284, 290, 282 in the confinement cavity, as 5 explained below. The transistor depth (thickness) is well controlled by the thickness of the semiconductor membran 280 which in turn can be precisely determined by epitaxial and/or etching means.

The exposed semiconductor film 280 is then 10 anisotropically etched back in two directions under the dielectric over layer 290 and along the isolation trenches 284 as shown in Figure 12c. This forms a very smooth walled confinement cavity 292 with a smooth seed crystal 292-a, 292-b at the end of the cavity 292. The etch is 15 stopped at a lateral depth consistent with the design requirement for the number of transistors to be formed in the confinement cavity. The depth "c" of the confinement cavity 292 may vary from about 2 μm to over 15 μm .

A smooth contamination free seed crystal wall 292-a, 20 292-b is required for the subsequent epitaxial growth. The crystal seed wall 292-a, 292-b will form at an angle dependent upon the crystallographic orientation of the semiconductor film. A $<100>$ silicon film will form a seed wall angle of approximately 54.74° as measured from the 25 horizontal, and a $<110>$ silicon film will form a seed wall 292-a, 292-b with an angle 90° (as shown in Figure 12c). GaAs and InP have similar crystallographic properties and can be used as the semiconductor film instead of silicon.

The selective epitaxial growth of crystalline 30 semiconductor proceeds from the seed crystal wall 292-a, 292-b. The npn or pnp regions of silicon MOSFET transistors are epitaxially grown (see Figure 12d) with in situ doping to whatever design thicknesses desired. This allows the length of the base or gate region of the 35 transistor to be determined by the epitaxial growth

process instead of a lithographic process as presently done. This also allows the length of the base or gate region of the transistor to be arbitrarily narrow, which cannot be done with current lithography methods. Figure 5 12d shows the confinement cavity 292 filled with a CMOS transistor pair of npn and pnp structures 294, 296. Each region of the transistor can be uniquely tailored to length and doping concentration level, in addition, because the transistor channel is formed by epitaxial means, doping of the transistor 294, 296 regions, can be extended to graded segments as discussed above. Further, non-symmetric doping of source and drain regions can easily be implemented by time based selection of dopant during epitaxial growth; this is not easily accomplished 15 in bulk wafer processing due lithography limitations in resolving the gate region.

Figure 12d shows two pairs 294, 296 of CMOS transistors formed as mirror images of each other in two confinement cavities; this was a design choice because a 20 single confinement cavity could have been formed by additional trench dielectric isolation of the initial confinement window opening. Depending on the method of epitaxial growth, gate region lengths "g" of less than 25 nm can be fabricated. In contrast, prior art MOSFET 25 transistor gate regions are predominately formed by optical lithographic means and are presently limited to minimum gate region lengths of approximately .5 μm (500 nm).

Figure 12e shows the CMOS transistor pairs 294, 296 30 with electrode contacts 294-a, 294-b, 294-c, 296-a, 296-b, 296-c. The isolated gate electrodes 300, 302, 304, 306 each span the narrower gate region length of the transistor. The gate electrode is formed by standard lithographic processes, and may be many times of greater 35 length than the gate region length of the transistor. For

example, a lithographically defined gate electrode of .5 μm and a transistor gate region length of 25 nm are possible. Gate electrode capacitance attributed to the gate electrode overlap of the source or drain regions can be reduced as described above with the GGD, EEG, and GEO methods. Figure 12f shows embodiments of all of these methods; the electrode 312 opposed to the gate electrode 308 is presented optionally as a substrate bias. Also shown in Figure 12f are source region 294-1, optionally graded doped gate region 294-2, epitaxially extended gate regions 294-4, offset gate electrode 308, gate isolation 310, and optionally epitaxially extended substrate 312-a.

The MDI Confined Lateral Epitaxy method is not limited to MOSFET transistors or silicon as a semiconductor material. The MDI Confined Lateral Epitaxy method can be used to fabricate silicon bipolar transistors, or applied to other semiconductors such GaAs or InP which can be epitaxially formed. An example of a bipolar transistor is shown in Figure 12g when emitter region 314, base region 316, epi-extended base and electrode 318, collector 315, and optionally epi-extended base and electrode 319.

The semiconductor layer of a MDI circuit membrane provides various methods to pack circuit devices densely, mix semiconductor types or simplify the fabrication steps. Figures 12h, i & j show examples of such methods. Figure 12h shows a silicon membrane 289 upon which an epitaxial dielectric 291 and a subsequent layer of epitaxial semiconductor 293 has been formed; the total thickness of this membrane structure is typically less than 4 μm . The dielectric layer 291 should closely match the crystal lattice dimension and structure of the silicon 289; an example of such a dielectric with a similar crystal lattice is sapphire or undoped silicon under certain device design parameters. This MDI semiconductor layer

structure allows semiconductor devices to be formed on either side of the semiconductor layer 289 and remain electrically isolated. An obvious application for this semiconductor or membrane structure is CMOS integrated circuits with p-type device formed on one side and n-type devices formed on the opposite side. Low stress dielectric would be used to^{trench} isolate individual semiconductor devices and complete the MDI process suggested by Method #2. Further, the second epitaxially grown semiconductor layer 293 can be a material other than silicon such as GaAs or InP.

Figure 12i shows a MDI circuit membrane composed of a silicon layer 295 and a low stress dielectric layer 297. The dielectric layer 297 has been patterned to form open areas 299 into which semiconductor material was deposited by selective epitaxial growth. The selectively deposited semiconductor 299 can be an semiconductor other than silicon, or silicon. Semiconductor devices can be fabricated in the epitaxial islands 299 on the backside of the MDI semiconductor layer.

Figure 12j shows a MDI circuit membrane composed of a silicon layer 295 and a low stress dielectric layer 297. The dielectric layer 297 has been patterned and silicon islands 299 formed through selective epitaxial growth in the same manner as described for Figure 12i. The silicon layer 295 was subsequently patterned removing portions of the silicon layer opposite each island 299 that was epitaxially grown in the dielectric layer, and then filling with low stress dielectric. Circuit devices formed in the semiconductor islands 299 are dielectrically isolated. This membrane structure has similar applications as those suggested for Figure 12h.

The structures Figures 12h, i & j show that a two level device structure can be formed that permits more compact interconnection of the circuit devices by the use

of vertical interconnections. These structures also simplify the fabrication of mixed device technologies such as BiCMOS by allowing the Bipolar and MOSFET devices to be fabricated on either side of the semiconductor membrane 5 without an increase of interconnect complexity. The use of these MDI structures typically doubles the total surface area available for interconnect metallization routing. The obvious potential processing benefits can be a reduction in the number interconnect metallization 10 layers per side and or relaxation of the interconnect metallization pitch used, both of these benefits normally lead to an increase in circuit yield.

Dielectric Membranes as Sensor on Rigid Substrates

The mechanical (physical) and thermal properties of 15 the nitride and oxide free standing membranes made with the Novellus equipment are similar to silicon membranes presently being used in the making of ICs with integrated sensors. Examples of such silicon membrane or diaphragm based sensors are those made for sensing acceleration, 20 pressure or temperature, but not limited to these areas. The availability of such oxide and nitride dielectrics for general application is novel with this disclosure.

The use of such free standing dielectrics membranes significantly reduces the complexity of producing a 25 membrane with non-conducting properties in a silicon or semiconductor fabrication environment. The low stress dielectric membranes have selective etchants that allow the dielectrics to be processed independently in the presence of silicon. The known passivating capability and 30 inert chemical nature of silicon nitride, and the relatively similar coefficient of thermal expansion of silicon, silicon dioxide and silicon nitride increases the operating environmental range of sensors versus organic dielectrics.

Sensor diaphragms of low stress dielectric membranes produced on rigid substrates (typically semiconductor) can in most cases directly replace silicon membranes or be used in conjunction with a silicon membrane formed on a 5 rigid (conventional) semiconductor substrate. No new fabrication methods are required to integrate the low stress MDI process dielectrics into such sensor ICs.

APPLICATIONS OF MDI CIRCUIT MEMBRANES

The following discloses additional applications of 10 the MDI process, and of forms of MDI circuit membranes and extensions of the MDI IC process. For example, a MDI circuit membrane with few or without active circuit devices is called^{more specifically} an interconnect circuit membrane. When the interconnect circuit membrane is used to interconnect 15 conventional ICs in die form, the interconnect circuit membrane becomes a multiple chip module (MCM) interconnect circuit membrane as discussed immediately below. This does not limit the application of a MDI circuit membrane with active and passive circuit devices from being used in 20 the fabrication of a MCM.

1964

MDI Multi-Chip Module Interconnect Circuit Membrane

A MDI circuit membrane composed primarily of interconnect metallization of one or several internal interconnect levels can be fabricated on a substrate to 25 provide electrical interconnections between the bond (signal) pads of various individual dice (ICs) as in the well established packaging technique called multiple chip module (MCM). A MDI circuit membrane made for this type of application is called multi-chip module Interconnect 30 Circuit Membrane (ICM).

The multi-chip module interconnect circuit membrane is formed using the MDI process and conventional semiconductor processing techniques. The interconnect

circuit membrane may have several thousands of die metal bond pad contacts or bonding points. The position of these metal contact or bonding points on the surface of the interconnect circuit membrane can be arbitrarily placed.

The multi-chip module interconnect circuit membrane can be formed on any substrate material that can meet the requirements for flatness specification, withstand the processing temperatures of the applied low stress dielectric(s), and can be selectively etched with respect to the low stress dielectric(s) to form the circuit membrane. Figure 13a shows an embodiment of an multi-chip module interconnect circuit membrane made as described above by the MDI methods. Figure 13a includes the interconnect circuit membrane 320 with several internal metallization trace layers (not shown), ICs (dice) 322a, 322b, 322c, interconnect circuit membrane substrate frame 324, and IC bonding contacts 326. Figure 13b shows a related structure which is a cross-section of a functional tester for testing ICs with probe points 330 formed on attached ICs 336a, 336b.

The interconnect circuit membrane can also be formed (see Figure 14) using the MDI method on a quartz substrate 340 that has been coated with a release agent such as KBr; this assumes that a single-crystal type membrane or substrate 340 is not required for the fabrication of various types of active circuit devices (SDs) in the interconnect circuit membrane 320. Thus this structure is made as described above, but without monocrystalline SDs, as in a MCM that as a minimum requires only an interconnect circuit membrane or passive circuit devices and transistors made from polycrystalline or amorphous semiconductor. Figure 15 shows the multiple chip module interconnect circuit membrane 320 of Figure 13a made with the release agent method of Figure 14 and

held by a separately formed frame 350 that was bonded to the interconnect circuit membrane 320 just prior to activating the release agent by scribing at the shoulder of the quartz substrate, thereby cutting through the 5 interconnect circuit membrane 320 and applying the appropriate solvent for the release agent. The array of die (ICs) 322a, 322b, 322c can then be directly bonded (as described below) to the interconnect circuit membrane 320, or the interconnect circuit membrane 320 can be aligned 10 and mechanically held against the pads of the surfaces of the array of die (ICs) 322a, 322b, 322c to achieve electrical contact. Alternately, the circuit membrane made with the method utilizing polysilicon as disclosed above and shown in Figure 1j can also be used as an 15 interconnect circuit membrane to achieve a similar result as that shown in Figures 13a, 13b and 15.

The interconnect metallization traces in the circuit membrane form electrical connections from one or more of the contact pads of an IC to one or more contact pads of 20 the other ICs. The diameter of these pads can vary from less than 0.5 mil (.001" or 25 μm) to several mils. The limiting factors of the size of the IC contact pads is the lithography method used in fabrication and the assembly method; the cost of such methods increase as pad diameters 25 less than 3 mils are employed.

A die can be bonded to a circuit membrane with any of several techniques. Techniques such as compressive metal to metal bonding with such metals as Indium or gold (or their respective alloys), infrared thermal bonding, laser 30 bonding, and vertically conductive adhesive films such as ZAF from 3M Corporation are examples. Figure 16a shows the packaging for a version of the structure shown in Figure 13a, including IC carrier lid 352, compressible material (such as silicone) 354 attached thereto, carrier 35 substrate 355 of the MCM package, contacts 356 to th

carrier signal pins 357. An alternative package is shown in Figure 16b, with gastight gasket 358 enclosing pressurized volume 359.

If the interconnect circuit membrane 360 (see Figure 5 17a) is made from optically transparent dielectrics such as low stress silicon dioxide and or silicon nitride, this permits the conventional die (IC) 362 to be visually aligned on the interconnect circuit membrane 360 from the backside or from the side of the interconnect circuit membrane 360 opposite that of the die 362. A locally directed infrared or other heat source (not shown) can then be applied from the backside of the interconnect circuit membrane 360. On the opposite side (top side) is formed MDI pad 365 which is surrounded by solder wells 15 364, and solder weld bonds can be formed between the interconnect circuit membrane pads 365 and the die bond pads 366 on which is formed solder bump 367 which typically is about 5 to 25 μm thick. The die 362 is attached face down against the interconnect circuit 20 membrane 360.

Solder weld bonds are formed by using a heat source (not shown) such as a high intensity lamp, laser or metal instrument that can heat the solder to its melting point. The heat source melts the solder 367 (see Figure 17b) 25 directly under the die pad 360 by heating through the interconnect circuit membrane 360 while the die is in contact with the interconnect circuit membrane. The high temperature tolerance of the dielectric material, its innate elasticity and thin structure allow heat from the 30 heating source to quickly reach and melt the solder 367 to form a bond of 3 to 10 μm thickness. The melted solder 367 wets both the die pad 366 and the interconnect circuit membrane pad 365, and when it cools the solder 367 contracts holding the die pad 366 firmly against the 35 interconnect circuit membrane pad 365. The solder bond is

formed with no more pressure than what would be exerted when the die 362 is brought in contact with the interconnect circuit membrane 360, pressing into the interconnect circuit membrane and deflecting it by less than 25 μm . When the solder 367 is melted, the interconnect circuit membrane 360 assumes a uniform planar contact against the surface of the die 362. This also removes the requirement that the solder on each pad be formed to an exacting equivalent height.

10 The solder 367 (see Figure 17c) alternatively is originally electroplated onto the interconnect circuit membrane bond pad 365. The solder 367 is electroplated to a height between 5 and 25 μm . The original height of the solder bump 367 is greater than the depth of the solder well 364 of the interconnect circuit membrane 360 in which the pad 365 of the interconnect circuit membrane 360 is positioned. Figure 17b shows the structure of Figure 17c after soldering or bond formation. If a die is removed some excess solder 367 will remain on the pad 365 of the 20 interconnect circuit membrane 360. When a replacement die is bonded to the same interconnect circuit membrane pad, any excess solder will flow or be pressed into the solder well 364 and not prevent the surface of the die 362 and interconnect circuit membrane 360 surface from achieving 25 uniform firm contact with each other. A hermetic seal can be formed between the surface of the die 362 and the interconnect circuit membrane 360. This is done by forming a metal bond along all edges of the die (not shown). This bond can be soldered, and is formed as 30 described below.

An advantage of the high temperature tolerance of the interconnect circuit membrane which allows die solder bonding to be done without the application of any significant contact pressure between the interconnect 35 circuit membrane and die, is the ability (see Figure 18

showing a top view of bond pads on a die) to place die bond pads 370-1, 370-2, ..., 370-k, ..., 370-n directly over the circuit structures of the die (not shown). This allows the placement of semiconductor devices directly under a bond pad 370-k without concern that the semiconductor devices will be damaged, which is the case when mechanical wire bonding equipment is used to wire bond a die to its carrier. Damage-free bonding is not presently possible with current die wire bonding techniques, because such bonds are compressively formed with a mechanical arm which presses, rubbing through the die bond pad into the substrate of the die to be placed anywhere on the surface of the die. The MDI method makes the design of the IC easier, removes the need for reserved pad area on the die (which saves 5 to 10% of the surface area of the die) does not restrict the placement location of the pad, and allows the pads to be larger since area under the pads is no longer reserved exclusively for them.

A hermetic seal bond pad 372 extends continuously along the perimeter of the surface of the die. A hermetic seal of the surface of the die with the surface of the circuit membrane can be accomplished by the formation of an enclosing solder bond (comprising a solder well as described above for forming pad bonds) along the edge of the die. The hermetic seal is typically also a ground contact for the die.

The infrared solder bonding of die to the multiple chip module interconnect circuit membrane is a simple process which also allows the dies to be easily removed and replaced without damage to the interconnect circuit membrane. As shown in Figure 19a, the IC 372 is held by a vacuum tool 373 and aligned in close proximity to the MCM interconnect circuit membrane 374. Once aligned, the interconnect circuit membrane 374 is gently urged forward

by a fluid pressure 376 a distance of several mils and the die 372 is urged toward the interconnect circuit membrane 374 until contact is established. The infrared heat source 377 is applied to achieve localized heating of the 5 solder pads (not shown) on the IC die 372 until they melt and wet to the interconnect circuit membrane 374.

The die 372 can be removed (see Figure 19b) by using the same vacuum tool 373 to gently pull on the IC 372 while localized heating from heat source 377 of the IC is 10 applied until the solder bonds melt and the IC 372 can be pulled from the interconnect circuit membrane 374; no fluid pressure is applied to the interconnect circuit membrane 374.

The multi-chip module interconnect circuit membrane 15 can be enhanced to include passive devices such as resistors, capacitors, and polysilicon or a-Si (amorphous-silicon) TFTs (Thin Film Transistors). Such circuit elements can be fabricated into or onto the membranes due to the ability of the dielectric membranes to tolerate 20 processing temperatures in excess of 400°C. These circuit elements can be fabricated internally to the interconnect circuit membrane structure as part of various specific layers or collectively on either external side of the interconnect circuit membrane. After the interconnect 25 circuit membrane is freed from the substrate on which it is initially formed, it is strong enough to withstand continued semiconductor processing steps.

The multi-chip module interconnect circuit membran can further be enhanced to include any degree of active 30 single crystal semiconductor devices. This is consistent with the earlier discussion of the capability of bonding two or more MDI membranes to form a three dimensional IC, except in this case conventional dice (ICs) are bonded at the bond pads of the circuitry internal to a MDI circuit 35 membrane which is also serving the purpose of interconnect

circuit membrane.

The multi-chip module interconnect circuit membrane provides novel circuit cooling advantages due to its low mass structure. The thermal energy generation of an IC is 5 from the face side of the IC. ICs attached face down against the circuit membrane allows the thermal energy of an IC to be radiated and conducted through the circuit membrane to a liquid or solid heat sink means on the opposite side of the circuit membrane. The circuit 10 membrane provides a very short thermal path from the IC to the heat sinking means. The ability directly to cool ICs in this manner is a unique feature of the MDI interconnect circuit membrane structure. The cooling efficiency that 15 can be achieved by an IC that is fabricated with the MDI process as a circuit membrane is significantly improved versus standard thickness substrates by the obvious reduction in the thermal mass resistance of the semiconductor substrate.

Figure 13d shows in cross-section a portion of a MCM 20 MDI interconnect circuit membrane 329 including low stress dielectric and interconnect layer 329a and semiconductor layer 329b where two die 331, 333 are bonded face down at their signal pads 335a, 335b, 335c, 335d. The MDI circuit membrane 329 incorporates the pad drivers 337a, 337b, 25 337c, 337d that normally would be incorporated onto the die (IC). The primary advantages of integrating the IC pad drivers into the MCM are circuit performance, simplified use of mixed device technologies (Bipolar & CMOS), cooling and die size (IC real estate).

30 IC pad drivers are typically designed to meet a broad range of circuit design conditions which often results in a trade-off of performance. The designer of the MCM pad driver has a better understanding of the operational requirements of the pad driver, and therefore, can 35 typically optimize the pad driver design for higher

performance. Pad drivers in the MCM can be formed from Bipolar transistors while the IC can be CMOS. This achieves many of the benefits of BiCMOS without the fabrication complexity. The pad drivers of an IC typically generate more than half of the thermal energy of the IC especially at high operating speeds. Placing the pad drivers in the MCM provides a means to bring the primary thermal components of an IC into direct contact with heat sinking means. IC pad drivers are typically the largest transistor structures making up the IC. Moving the pad drivers of the IC into the MCM can result in a potential 5-10% reduction in the size of the overall IC.

The incorporation of low complexity ICs into a MCM MDI circuit membrane can reduce overall MCM assembly and parts costs. Such often used circuits as bus drivers or combinatorial logic can be incorporated into a MCM reducing parts and assembly costs without a corresponding increase in the cost to fabricate the MCM. (Once the decision has been made to include such circuits in a MCM MDI circuit membrane, there is no significant cost difference between the inclusion of 1,000 transistors or 10,000.) Yield of circuits in a MCM circuit membrane can be addressed through redundant fabrication of the desired circuit devices; the circuit devices of the MCM circuit membrane comprise only a small amount of the total surface area, typically less than 10%. The circuit devices of the MCM circuit membrane can be tested for defects. A MDI functional tester membrane disclosed herein, can be used to perform this testing and, in the same step if so desired, to blow anti-fuses to enable the defect free circuits or fuses to disable the defective circuits.

The multi-chip module interconnect circuit membrane, like prior art PCBs (printed circuit boards), can provide access to the contact pads of the IC from the opposite side on which the IC is attached. This access permits in-

circuit testing of the bonded IC to be performed by a separate interconnect circuit membrane fabricated to do such a functional test, and also permits electrical continuity testing of the traces fabricated in the multi-chip module interconnect circuit membrane, again performed by an interconnect circuit membrane test surface fabricated for that purpose. Figure 20 is a top side view of an interconnect module showing an interconnect circuit membrane surface bond pad 380 and interconnect circuit membrane feed-through contacts 382 from the bond pads of the dice 386-1, 386-2, 386-3 mounted by compression or solder bonding (see Figure 21) on the backside of the interconnect module of Figure 20. Also shown in Figure 21 are the backside 388 of the etched silicon substrate and the interconnect circuit membrane surface 190 with the traces 392-1, 392-2, 392-3 interconnecting the dice 386-1, 386-2, 386-3.

The multi-chip module interconnect circuit membrane method could also be used to construct a functional IC tester surface with a high number of probe points (in excess of several thousand) for testing ICs while in wafer or die form (i.e., wafer or die sort testing), and also to wafer sort subsections of ICs such as an ALU (Arithmetic Logic Unit), FPU (Floating Point Unit), cache segment, etc.

A functional circuit membrane tester surface made with the MDI process offers advantages not presently available from present on-wafer IC membranes testers constructed from polymers such as continuous high temperature operation (greater than 100°C) without deleterious effects due excessive material expansion or at-speed IC testing without EM interconnect trace coupling.

High numbers (in excess of 1000) of pads or traces of an IC or IC subsection can be contacted. The contact

sites of the IC (die) can be arbitrary in position and all sites can be contacted at one time. The contact sites (pads or traces) can be less than 50 μm (2 mils) or even less than 2 μm in diameter. The probe points of the 5 functional tester surface can be less than 50 μm or even less than 1 μm in diameter, and can be placed on center to center distances of less than twice the diameter of the probe points. (Functional probe points can be formed to be 12 μm in diameter and spaced on center to center 10 distances of less than 24 μm .) The ability to form and contact high numbers of pads or traces with dimensions smaller than presently available in the industry is due to the ability of the MDI IC process to form multiple layers of interconnect with established semiconductor fabrication 15 means resulting in a flexible and elastic membrane structure. The multiple layers of interconnect provide for denser contact test sites, the thin membrane structure provides for contact conformation with little required force (typically less than 10 psi), and the compatibility 20 of the dielectric material with standard IC fabrication techniques allows contact of contact site dimensions less than 2 μm .

A MDI circuit membrane 332 used as an IC functional tester surface extends under fluid pressure "P" to make 25 contact with the surface of a wafer or single die 339 to be tested as shown in Figure 13c. The MDI circuit membrane 332 can be formed with diameters of approximately the size of the substrate on which it is formed and to be extended more than 40 mils (0.1 cm) depending on the 30 diameter of the membrane. Probe points 330 on the tester surface are not restricted in size, and can range in size from greater than 4 mils (0.01 cm) to less than 2 μm in diameter. The number of probe points 330 can vary from less than 100 to several thousand without restriction and 35 the placement of the probe points can be arbitrary. These

capabilities of the functional tester surface are primarily due to the structural formulation of the materials used and the fabrication methods of the MDI process. The MDI functional tester surface can rub 5 through the native aluminum oxide layer of the bonding pads of the die 339 being tested by laterally moving the wafer or die 339 holding mechanism several microns (typically less than 10 μm) in a back and forth motion. This is uniquely facilitated by the durability of the 10 circuit membrane, the surface flatness of the membrane, the uniformity of probe point height and the low pressure required to extend the membrane surface so that all probe points are in contact with the substrate.

In the case of sub-section testing of a die, the 15 detection of a defective sub-section before packaging permits the option of pinning-out the IC as one of several alternative product configurations, and thereby, making useable an otherwise scrapped IC.

In Figure 13b the multi-chip module interconnect 20 circuit membrane has signal pad probe points 330 formed on the side opposite of the attachment of dice 336a, 336b. The dice 336a, 336b of the multiple chip module provide functional test signals to the probe points 330. The testing performed by the multiple chip module can be 25 functional testing of a whole die or a subsection of the IC. The probe points 330 are aligned over a die (not shown) to be tested on a wafer, and the interconnect circuit membrane 332 is extended several mils (nominally 15-30 mils) by a fluid pressure as shown in Figure 13c. 30 The wafer is raised to make contact with the probe points 330, the functional test performed, the wafer is lowered, positioned to the next IC (die location on the wafer) and the functional test repeated until all the ICs on the wafer have been tested. Testing die in this manner can 35 also be done on die that has already been cut from a

wafer. This is done by aligning and holding the individual die in contact with the probe points and the functional test performed. Piezoelectric horizontal vibration applied to the interconnect circuit membrane 332 or the wafer or individual die while the functional testing is being performed can be used to rub through native metal oxide on the die pads.

Alternately the native metal oxide (approximately 30Å thick) on the pads of a die can be rubbed through by 10 the probe points of the functional tester surface by repeatedly moving the wafer or die several microns in a lateral manner when the tester surface is first brought into contact with the IC to be tested. The mechanical control presently available with most wafer or die 15 handling equipment is sufficient to effect this rubbing action.

The interconnect circuit membrane can range in thickness from less than 2 μm to over 25 μm . A typical thickness per layer of interconnect (dielectric and metal 20 traces) is 1 to 4 μm . Dielectric layer of several microns thickness may be used as a planarizing technique to lessen metal trace step height differentials that can develop when more than two interconnect layers are used.

Planarization of metal traces can also be achieved by 25 depositing the dielectric to a thickness inclusive of the metal trace. A channel that is at least as deep as the desired thickness of the metal trace is patterned in the dielectric. Then established lift-off techniques are used to fill the channel with metal.

30 Figures 22a to 22c show this process. In Figure 22a, a portion of the interconnect circuit membrane dielectric 400 is shown with patterned resist layer 402 overlying. Recess 406 is then formed in dielectric 400 by isotropic etching to form undercut portions 404 equal nearly to the 35 depth of etched recess 406. In Figure 22b metal layer 408

is deposited. In Figure 22c lift off stripping of resist 202 is performed leaving only metal trace 408, and the next dielectric layer 410 is deposited.

Planarization of the interconnect structure can be 5 achieved by applying a thick layer of a planarizing polymer over the MDI dielectric film. The polymer must have an etch rate similar to that of the MDI dielectric film. The polymer is then removed completely by dry etch means and in the same process removing any dielectric 10 surface features that extended into the polymer layer.

This planarization process is identical to the optional planarization process disclosed in the process steps for the Air Tunnel. The only differences being the material being planarized is a MDI dielectric and not a-Si.

15 The ability of the interconnect circuit membrane to achieve reliable contact on the bond pads of a die (see Figure 13b) is strongly influenced by the thickness of the interconnect circuit membrane 332 which contains the probe points 330 for contacting the die to be tested. An 20 interconnect circuit membrane 332 may be 25 μm thick or more as required for example by transmission line design considerations of interconnect traces. Interconnect circuit membrane thickness at the probe points is preferably less than 8 μm . The structure of Figure 13b 25 can be fabricated as shown in Figures 23a and 23b.

In Figure 23a an etch stop layer 412 (typically metal) is deposited at a certain thickness of the interconnect circuit membrane 332 as the interconnect circuit membrane 332 is fabricated from repeated 30 applications of dielectric and metallization layers to a thickness of 8 to over 25 μm . After the fabrications of the interconnect layers of the interconnect circuit membrane 332 is completed, an area over the probe points 330 is masked and etched to the etch stop layer 412 (see 35 Figure 23b). The etch stop layer 412 is then etch

removed. Alternatively, the area 414 over the probe points 330 can be etched free of overlying interconnect layers as each layer is itself patterned as part of the fabrication of the interconnect metallization. Then dice 5 336a, 336b are attached to the interconnect circuit membrane 332.

MDI Source-Integrated Light Valve (SLV)

Direct Write Lithography Tool

The MDI process technology can be used to fabricate a 10 circuit membrane with an $n \times m$ cell array of active radiation sources of X-ray, DUV (Deep Ultra Violet) or E-Beam sources that can be used to form lithographic patterns in a film of appropriately sensitive resist. The preferred embodiment in this disclosure uses a X-ray 15 source. Variations of the electrodes, gas contents and structure of the radiation source cell can be made within the overall structure of this source integrated light valve embodiment. The preference for the X-ray source embodiment is its capability to pattern a smaller feature 20 size.

The radiation source cells in the membrane are under computer control, so that this type of MDI membrane combines the functions of reticle or mask and a light or radiation source for fabricating ICs. The radiation 25 source cells of this MDI circuit membrane are positioned (aligned) over an area of the substrate to be patterned and at a uniform distance from or in contact with the substrate. Each cell then illuminates (exposes) various portions of the substrate directly beneath it as required. 30 The MDI circuit membrane functioning in this manner is called herein a Source-Integrated Light Valve (SLV) and can generally be categorized as a Direct Write (maskless) Lithography Tool.

The array of Radiation Source Cells (RSC) that make

up the patterning structure of the SLV, emit a collimated source of radiation. The exposure feature size of this collimated radiation source is dimensionally much smaller than the area the RSC occupies on the surface of the SLV.

5 The emitted collimated radiation source is referred to as the Radiation Exposure Aperture (REA). The SLV is moved in a scanning X-Y manner over the substrate to be patterned. The dimensions of the scanning motions cause each REA of an RSC to pass over a portion of the substrate

10 that typically is equal in area to the size of the RSC. The RSCs are operated in parallel, and the patterned areas on the substrate beneath each RSC adjoin each other and collectively form a much larger overall pattern on the substrate. This pattern can be as large as the underlying

15 substrate. The scanning motion of the RSCs is generated by well known computer controlled mechanical motor driven stages or piezoelectric driven stages. The SLV or the substrate can be attached to the motion stage. Due to the short X-Y motions in the use of the SLV, and the desire to

20 scan the RSCs with REAs of dimensions much less than 1 μm , and in some cases with dimensions of less than 50 nm, piezoelectric motion stage drive is the preferred embodiment. As the REAs of the SLV circuit membrane are scanned over the substrate, they are turned on or off by

25 computer controlled logic associated with each RSC to effect the desired exposure pattern to be made on the surface of the substrate. An example would be a RSC with an area of 25 μm by 25 μm and a REA of .1 μm in diameter.

In order for the REA to expose an area the size of the

30 RSC, a scanning motion of 25 μm by 0.1 μm would be made 250 times in the X-axis direction while translating 0.1 μm in the Y-axis direction after each scan.

Figure 24 shows an overhead (plan) view of a prototypical SLV 420 with an array size of 4,096 by 4,096 RSCs, and an overall size of approximately 5 inches by 5

inches. The SLV array 420 of RSCs has associated control logic 424 for loading the pattern data to each RSC. The SLV 420 (including the control logic 424) is a MDI circuit membrane of nominally 8 μm to 50 μm in thickness made by 5 established semiconductor processes and held in a rigid frame 426 made from the original substrate on which the SLV 420 was fabricated or a frame bonded to the SLV prior to the selective etch removal of the substrate on which the SLV (MDI circuit membrane) was fabricated.

10 Electromagnetic coupling alignment structures 430 (described below) are shown also.

Figure 25 shows a cross-section of two RSCs 434-1, 434-2 in a SLV 440. A SLV 440 in the preferred embodiment has rows and columns of RSCs 434-1, 434-2 where each row 15 and each column can include more than 1,000 RSCs resulting in a total count of RSCs in a SLV in excess of several million. Figure 25 shows a MDI circuit membrane 440 which is 8 to 50 μm thick, data bus interconnect metallization 442-1, 442-2, control logic 424-1, 424-2, X-ray sources 20 446-1, 446-2, and REAs 434-1a, 434-2a.

Figures 26 and 27 are cross-sections of two different potential implementations of X-ray RSCs 434. Figure 26 uses a metal cathode 450 with a highly textured surface 452 in the shape of adjacent cubes; each corner of the 25 extended portion of each cube is a cold electron point emitter which emits electrons into the electric field 456 created by the high voltage x-ray emitting target 458 beneath it. The size of the RSC 434 is approximately 25 $\mu\text{m} \times 25 \mu\text{m}$. The thickness (height) of the RSC 434 is 30 approximately 8 to 50 μm . The materials used to fabricate the SLV (and RSCs) are those employed to fabricate a MDI circuit membrane as described above -- metal 459, low stress dielectric 460 and a single crystalline semiconductor membrane substrate 472. The processing 35 steps can vary widely, but are those used in conventional

semiconductor and micro-machinery fabrication.

The textured cathode 450 will typically be in the shape of a square array of rows and columns of metal cubes, with each cube having dimensions much smaller than 5 the overall dimensions of the square cathode layer. As an example, if the cathode 450 is $4 \mu\text{m}^2$ in area, the dimension of each cube would be .1 to .5 μm on a side. The textured cathode cubes are made by established lithography techniques (E-Beam or DUV optical lithography) and 10 anisotropic RIE processing. This cathode 450 configuration is a novel part of the SLV because of high density of cold electron emitters, and therefore, high electron fluence onto the anode 458. The cathode 450 emits electrons which are accelerated by the electric 15 field 456 created by the voltage potential of the target or anode 458. When electrons reach the target 458, X-rays are emitted from the target 458. X-ray absorber materials 466 such as tungsten or gold are deposited as layers as part of the fabricated structure of the SLV membrane to 20 provide a means to form the REA 470 and in back scatter layer 461 to prevent back scattered X-rays from reaching control logic devices 472 with interconnect 473 to other RSCs in the SLV. This RSC is related to the well known 25 X-ray vacuum tube design. The space 474 separating the cathode and target is in partial vacuum. This separation distance can vary from less than 1 μm to 40 μm .

Figure 27 shows an alternative RSC 434 that uses a laser diode 480 to irradiate onto a target 458 which in turn emits X-rays. The laser diode 480 and the target 458 30 are separated by a distance "d" of 1 or more microns in a cavity 482 that is optionally a partial vacuum. Except for the technique of inducing the emission of X-rays from the target 458 material, the RSCs 434 shown in Figures 26 and 27 are functionally the same. RSCs that employ gases 35 such as Cd-Hg or Xe-Hg as in the case of DUV radiation

sources, the structure of the electrodes in the cavity of the RSC would change and X-ray absorber layers would not be necessary. RSCs that emit free electrons for resist patterning would require that the REA 470 be an opening or 5 that it be closed by a material thin enough to allow the accelerated beam of electrons to pass through it. If the REA 470 is an opening from the electrode cavity 482 of the RSC, then the SLV would have to be operated in vacuum, just as is the case with E-Beam lithography tools. The 10 Hampshire Corporation (Marlborough, MA) presently manufactures an X-ray lithography tool which uses a laser diode stimulated X-ray radiation source.

Although laser diodes that emit radiation with a wavelength less than approximately 6,000Å do not presently 15 exist, development of shorter wavelength laser diodes is on-going and contemplated as a radiation generator for the SLV. There is significant demand for diodes with shorter wavelengths for use in consumer and computer peripheral products like compact discs. Such devices in the not too 20 distant future may come into existence and such laser diodes could possibly be integrated into the SLV as a radiation source generator of a RSC. The use of laser diodes is therefore contemplated. An additional application of the SLV (with a RSC of appropriate 25 radiation capability) is radiation-induced CVD (chemical vapor deposition). The use of an SLV in this manner eliminates the need for mask and etch processing steps. The material of interest to be deposited, be it metal or dielectric, is deposited in a patterned form. This 30 provides for a maskless, resistless, etchless process and it has significant cost and particulate contamination advantages. The SLV operating in this manner supplies radiation at the surface of a substrate where a mixture of gaseous compounds are present. This process step is 35 mechanically the same as exposing a resist layer on the

substrate as discussed above. The radiation from a RSC causes the compounds to react at the surface of the substrate leaving a deposition of material selectively on the irradiated portions of the surface of the substrate.

5 This method of radiation-induced selective CVD has been demonstrated with the use of excimer lasers. Laser diodes that can emit radiation in the excimer frequency band of 75 to 250 nm do not presently exist.

MDI Source-External Particle Valve (SPV)

10 Direct Write Lithography Tool

The MDI process technology can be used to fabricate a circuit membrane with an $n \times m$ cell array of individually controlled electro-static or electromagnetic valves or shutters. These valves can be used to control the passage 15 of charged particles through the circuit membrane to create an exposure pattern in a film of appropriately sensitive resist. The array of valves on the MDI circuit membrane is for practical purposes the same structure as the SLV structure shown in Figure 24. The primary 20 difference is the use of particle valve cells for patterning an external particle source which illuminates one side of the SPV circuit membrane, instead of a cell with an integrated patterning source as in the case of the SLV lithography mask.

25 The array of valve cells of this MDI circuit membrane is placed between a collimated ion particle source and at a uniform distance from or in contact with a substrate coated with a thin film of resist. The array is positioned (aligned) over an area of the substrate to be 30 patterned and the array of valves, under individual computer control, allow ion (charged) particles to expose or not expose an area of resist coated substrate directly under beneath it. The MDI circuit membrane functioning in this manner is called herein a Source-External Particle

Valve (SPV).

The collimated particle beam passed by a particle valve has a fixed exposure feature size called the Particle Exposure Aperture (PEA). The SPV is moved in a scanning X-Y manner over the substrate to be patterned.

The dimensions of the scanning motions cause each PEA of a particle valve to pass over a portion of the substrate that typically is equal in area to the size of the valve. The valves are operated in parallel (simultaneously), the patterned areas on the substrate beneath each valve adjoin each other and collectively form a much larger overall pattern on the substrate. The scanning motion of the valves is generated by well known computer controlled mechanical motor driven stages or piezoelectric driven stages. The SPV or the substrate can be attached to the motion stage. Due to the short X-Y motions in the use of the SPV, and the desire to scan the valves with PEAs of dimensions much less than $1 \mu\text{m}$ in diameter and in some cases less than 50 nm, piezoelectric motion stage drive is the preferred embodiment. As the valves of the circuit membrane are scanned over the substrate, they are turned on or off by computer controlled logic associate with each valve to effect the desired exposure pattern to be made on the surface of the substrate. An example would be a valve with an area of $25 \mu\text{m}$ by $25 \mu\text{m}$ and a PEA of $0.1 \mu\text{m}$ in diameter. In order for the valve to expose an area the size of the valve, a scanning motion of $25 \mu\text{m}$ by $0.1 \mu\text{m}$ would be made 250 times in the X-axis while translating $0.1 \mu\text{m}$ in the Y-axis after each scan.

Figure 24 (also a plan view for the SLV) shows an overhead (plan) view of a prototypical SPV 420 with an array of 4,096 by 4,096 ion or charged particle valves, and an overall size of approximately 5 inches by 5 inches. The SPV array 420 of valves has associated control logic 424 for loading the pattern data to each valve. The SPV

420 (including control logic 424) is a MDI circuit membrane of nominally 4 μm to 8 μm in thickness made by established semiconductor processes and held in a rigid frame 426 made of the original substrate on which the SPV 5 420 was fabricated. Electromagnetic coupling alignment structures 430 (described below) are shown also.

Figure 29a shows a cross-section of two valves 502, 504 in a SPV 506. A SPV in the preferred embodiment has rows and columns of valves 502, 504 where each row and 10 each column can include more than 1,000 valves resulting in a total count of valves in a SPV in excess of several million. Figure 29a shows a MDI circuit membrane 508 which is 4 μm to 8 μm thick, data bus 510a, 510b, control logic 512a, 512b and PEA (aperture) 514a, 514b for passage 15 of ion particles. Figure 29b shows a plan view of the valves 502, 504 of Figure 29a.

The valves of the SPV prevent the passage of ions or charged particles by using an electric or magnetic field of the same polarity to deflect approaching particles from 20 the PEA. The PEA 514a, 514b is typically a square opening in the SPV circuit membrane 508. The PEA 514a, 514b is circumscribed by a metal film 520a, 520b which creates a local electro-static field over the PEA by applying a voltage potential, or by a metal wire 540 (coil) (shown in 25 Figure 29e) which creates a local electromagnetic donut shaped field. When the SPV is flooded with a collimated source of charged particles, the particles that fall upon the PEA 514a, 514b will pass through the SPV 506 and continue onto the resist layer (not shown) to be patterned 30 directly beneath the SPV 506. If a electro-static field or electro-magnetic field of sufficient strength and of the same polarity as the ionic particle is present, the ionic particle will deflect away from the PEA and strike some other portion of the SPV surface. The PEA is small 35 in area relative to the total generated electric field

volume, therefore, only a small deflection of the approaching charged particle is required for it to miss the PEA and strike the surface of the SPV.

The SPV 506 is typically operated in an enclosure 5 (not shown) under vacuum. The charged ions or particles can be of any material that can be appropriately accelerated or caused to uniformly flood the surface of the SPV. Some examples of charged particles that have been used as sources for patterning resist films are 10 electrons (negative), protons (positive) and gallium+ (positive). The SPV can be in close proximity or contact with the substrate to be patterned, or it can be positioned before imaging lens elements of the lithography equipment that could be used to enhance the focus of the 15 particles beams formed by passing through the SPV circuit membrane or demagnify (reduce) the image generated by the SPV.

Figures 29c and 29d are cross-sections that show different methods for implementing an electro-static 20 shutter or valve of the SPV. Figure 29c shows a PEA 514a formed by an anisotropic etch of the monocrystalline semiconductor membrane 524; <100> monocrystalline semiconductor wet etches with a wall angle of approximately 54° or dry etching (RIE) methods can also be 25 used to etch a round or square hole to form the PEA 514a in either the low stress dielectric 526a, 526b or semiconductor layer 524 of the SPV circuit membrane. The via in the low stress dielectric membrane 526b on the backside of the semiconductor membrane was formed after 30 the wet etch of the PEA 514a. A thin metal film 528 of typically less than 2,000Å is deposited by sputtering or CVD means. The metal film 528 circumscribes the PEA 514a and has a diameter typically of less than 4 µm, and the PEA typically has a diameter d of less than 500 nm. 35 Figure 29d shows a PEA 530 formed by etching a via in a

flat metal film 532 that was deposited on the semiconductor membrane 534. The metal film 532 forming the PEA in this example is typically less than 2,000Å thick and has a diameter of approximately 4 μm . Also shown are low stress dielectric layers 536a, 536b.

Figures 29e and 29f show a method for implementing an electromagnetic shutter or valve of the SPV. Figure 29e is a plan view of the structure of Figure 29f. Shown are semiconductor membrane layer 542 and layer 544 low stress dielectric. A metal coil 540 is formed on MDI circuit membrane 508 so a current loop can be created around the PEA 514a. The PEA 514a is formed by wet or dry anisotropic etching in either the dielectric or semiconductor portions of the MDI circuit membrane 508. The metal line 540 is typically less than 2 μm wide, less than 1 μm thick and circumscribes an area "a" typically less than 4 μm in diameter. The PEA 514a is smaller than the inner diameter "a" of the loop of the metal line 540 and typically less than 500 nm.

Control logic is associated with each valve of a SPV, supplying voltage or current as necessary to the metal structure circumscribing the PEAs. In Figures 29c and 29d the valve control logic applies a voltage potential to the metal film 528, 532 respectively circumscribing the PEA. If the applied voltage potential is of the same polarity as the charge particles striking the surface of the SPV, the particles will be deflected from passing through the PEA. This is the valve closed condition. If the applied voltage potential is of the opposite polarity or zero, particles will pass through the PEA. In Figure 29e and 29f the valve control logic applies a current through the metal wire 540 circumscribing the PEA 514a. Depending on the direction of the current in the wire 540 (clockwise or counter-clockwise about the PEA) a magnetic field with a polarity is generated. If the field polarity is the same

as the approaching charged particle it will be deflected, and if the field polarity is the opposite or zero particles will pass through the PEA.

The design of electro-static or electromagnetic valves for achieving the desired functions of the SPV can vary widely. The examples presented here are not intended to limit the scope of the design structure of such valves for use in a SPV.

MDI Mechanical Light Valve (MLV)

10 Direct Write Lithography Tool

Figures 29g through 29k show portions of a direct write lithography tool which uses repeated micro-machined mechanical electro-static shutter cell 550-k for the patterning of photonic or particle exposure source. The overall structure and function of this lithography tool is similar to the above described SLV and SPV tools. It is composed of rows and columns of pattern forming elements called shutter cells 550-k that are each approximately 25 μm by 25 μm . Figure 29g is a plan view of several such cells 550-1, 550-2, ..., 550-k, ..., 550-n. Figure 24 represents a general plan view of the whole lithographic tool, which looks the same in plan as the SLV and SPV tools.

An array of shutter cells 550-k made on a MDI circuit membrane is placed between a collimated photonic or ion particle source and a substrate to be patterned, and can be used in projection or contact lithography methods to pattern such a substrate coated with a thin film of resist. The array is positioned (aligned) over an area of the substrate to be patterned and the array of shutter cells, each under individual computer control regulating the shutter opening or REA (Radiation Exposure Aperture) through the circuit membrane, exposes an area of the substrate directly beneath or corresponding to it. The

MDI circuit membrane functioning in this manner is called herein a Mechanical Light Valve (MLV).

The size of the REA collimated exposure image passed by a shutter cell 550-k is variable. Further, the REA 5 does not need to be a physical opening through the MDI circuit membrane for photonic sources, but only transparent to the incident photonic radiation. The MLV is moved in a scanning X-Y manner (shown by X-Y axis 554) over the substrate to be patterned. The dimensions of the 10 scanning motions cause each REA of a shutter cell to pass over a portion of the substrate that typically is equal in area to the size of the shutter cell 550-k. The shutter cells 550-k are operated in parallel (simultaneous) manner; the patterned areas on the substrate beneath each 15 shutter cell adjoin each other and collectively form a much larger overall pattern on the substrate. The scanning motion of the shutter cell is generated by well known computer controlled mechanical motor driven stages or piezoelectric driven stages. The MLV or the substrate 20 can be attached to the motion stage. Due to the short X-Y motions in the use of the MLV, and the desire to scan the shutter cells with REAs of dimensions much less than 1 μm in diameter and in some cases less than 50 nm, piezoelectric motion stage drive is the preferred 25 embodiment.

As the shutter cells of the circuit membrane are scanned over the substrate, they are opened or closed by computer controlled logic 556-k associated with each shutter cell 550-h to effect the desired exposure pattern 30 to be made on the surface of the substrate. An example would be a shutter cell with an area of 25 μm by 25 μm and a REA setting of 0.1 μm in diameter. In order for the REA to expose an area the size of the shutter cell, a scanning motion of 25 μm by 0.1 μm would be made 250 times in the 35 X-axis while translating 0.1 μm in the Y-axis after each

scan. The size setting of the REA is typically fixed for a given scan of the substrate, and vector motion of the REA can be used to improve exposure performance when there are areas of the substrate common to all shutter cells 5 that do not require exposure such as is the case with via pattern layers.

The operation of the shutter cells regulates the opened/closed status of an opening that allows a fluence of the exposure source (photons or particles) to pass, and 10 in the same operation dynamically determines the exposure CD for the lithography tool. The ability to change the minimum exposure CD or REA of the MLV is unique to this tool, versus the SLV and the SPV which have fixed exposure apertures. The ability to dynamically change the size of 15 the REA allows the pattern or geometry fracture database of the IC to be partitioned into CD specific geometry sets per pattern layer of an IC. This provides the capability to optimize the performance of the lithography tool by patterning those portions of an exposure image with the 20 smallest CD (processing rate is due to the size of the REA, therefore, the smaller the REA the greater the number of REA exposures), separately from other portions of the exposure image composed of larger CDs.

Figures 29h and 29i show plan views of two different 25 shutter arm structures of a shutter cell 550-k. Figure 29i shows a spring suspension structure of the shutter arm 560, 566. The shutter arm 560, 566 is formed of metal or a combination of metal and low stress dielectric and is suspended over the surface of the substrate from two 30 electrical contacts 562, 564 on either side of the shutter 566. The shutter arm 560, 566 can move (in the direction 570-Y indicated) by the switched application of electrostatic potentials. The REA 572 of the shutter cell is formed by the intersection of a square opening 574 through 35 the non-transmissive material of the shutter arm and a

similar opening through a metal electrode film directly below the central area of the shutter 566 and fixed to the surface of the substrate. This opening 574 is typically less than 2 μm in diameter, and is positioned with a 90° rotation relative to the long axis of the shutter arm 560.

Figure 29h shows in dotted outline 578 as an alternate position of the shutter arm 560, 566 produced by the application of electro-static potentials. The size of the REA is determined by the projected intersection of the 10 opening in the central area 566 of the shutter and the opening in the fixed metal film beneath it. The REA of the shutter 572 is closed by moving the central area of the shutter arm 566 a distance greater than the diagonal length of the square opening 574.

15 The shutter arm 560, 566 is positioned or moved by electro-static potentials. The shutter arm 560, 566 is provided with a voltage potential. Electrodes 580a, 580b positioned at either end of the maximum travel displacement of the central area of the shutter arm 566 20 are selectively set at opposite potentials sufficient to attract or repel the shutter arm a desired displacement. The shutter arm is held in physical contact with the electrode film beneath it by applying an opposite potential to the lower substrate electrode (not shown).

25 Figure 29j is a cross section of part of the shutter cell through line j-j of Figure 29h. Figure 29k is a cross section along line k-k of Figure 29j.

As shown in Figure 29j, the shutter cell is fabricated with established semiconductor processing methods. The array and shutter cell control logic are 30 fabricated on a MDI circuit membrane 590. A trench 592 is formed down to a lower dielectric layer 590 of the circuit membrane sufficient in size to accommodate the motion of the central area 566 of the shutter arm. The electrode 35 594 under the central area 566 of the shutter arm is

X

Sacrificial
formed, and a conformal ~~saerofinal~~ layer (not shown) of a-Si (amorphous Silicon) is deposited over the area of the shutter array. The thickness of the a-Si layer determines the separation distance that the shutter arm is suspended 5 above the circuit membrane. Into the a-Si layer via openings 562, 564 (Figures h and i) are patterned to the electrode contacts of the shutter arm 560 and to the electrode contacts of the shutter arm positioning electrodes 580a, 580b. A metal layer 600 optionally 10 combined with a dielectric layer 602 is deposited and patterned to form the shutter arm 560, 566 and the positioning electrodes 580a, 580b. The opening 574 that is used to form the REA is also patterned and etched via RIE processes. This opening 574 as a minimum passes 15 through the shutter arm and the electrode 594 below the central area of the shutter arm that is used in forming the cross-sectioned area that is the REA 572. The opening 574 may be completely through the MDI circuit membrane 590, or stop on the dielectric layer depending on the 20 transmission requirements of the exposure source. The a-Si is then selectively removed which leaves the shutter arm 560 free standing and connected to the circuit membrane at only two electrode contact sites 562, 564 (Figures h and i). The shutter arm 560, 566 is free to 25 move in two directions 570-Y, 570-Z based on the voltage potentials applied to the shutter arm 560, 566 positioning electrodes 580a, 580b, and the substrate electrode 594 beneath the central portion of the shutter arm.

Fixed Free Standing Membrane Lithography Masks

30 The MDI process can be used to form free standing membranes used as lithographic masks with fixed patterns. The MDI process can be used to form optical, X-ray and stencil masks (ion or charged particle masks). The mask substrate is made from a low stress dielectric and

optionally semiconductor material. In the preferred embodiment masks are made from oxide and nitride low stress dielectric made on the Novellus equipment and consistent with the formulation presented above or as variations of such low stress membranes formed on other oxide and nitride fabrication equipment. The patterning material is a semiconductor such as silicon, another dielectric material or a metal which is non-transmissive to a photonic exposure source. If the exposure source is an ion or charged particle beam, then the patterning is accomplished with voids (openings through the membrane) or a lack of material, or stencil.

Figures 291 and 29m show in cross-section the formation of a fixed photonic mask. A membrane substrate 620 initially formed of dielectric layers 622, 624 and silicon 626 (patterning material shown with pattern) is formed as described above. The thickness of the dielectric layers 622, 624 of the membrane is typically 2 to 3 μm thick, and the silicon 626 may vary in thickness depending upon the desired sidewall angle of the silicon or the CD aspect ratio (ratio of layer thickness to the CD opening of the pattern). The silicon layer 626 can be patterned directly with established resist spin-on films, pattern generation lithography tools such as E-beam and selective silicon etch processing.

Figure 291 shows in cross-section a patterned silicon layer 626 formed by first patterning an overlay of metal 630 such as tungsten, and then selectively etching the silicon layer 626 down to the dielectric layer 622. A metal pattern could also be formed by removing the silicon layer altogether and depositing a metal film, then subsequently patterning it, or by selectively undercutting the patterned silicon layer of Figure 291 to employ a lift-off process with a noble metal such as gold.

Figure 29m shows in cross-section the structure of

Figure 29l after the deposition of a low stress dielectric membrane layer 632 over the pattern and the removal of the dielectric layers 622, 624 below the pattern. The deposition of low stress dielectric membrane layer 632 over the pattern forms a structural membrane layer so that the original lower dielectric structural layers 622, 624 could be removed.

In the case of X-ray masks gold is often used as the patterning film because it is a good X-ray absorber. Gold and the noble metals in general can be patterned only with wet processing techniques and or in combination with electro-plating techniques. The silicon pattern 626 of Figure 29l can be dry etched (RIE) to achieve significant aspect ratios. If the silicon layer 626 is heavily gold doped prior to RIE processing, this method of mask formation can be used as an X-ray mask without CD feature size or aspect ratio limitations of wet etch processing.

Figure 29n and 29p show a stencil mask formed by patterning the dielectric layer 640 of a MDI silicon 642 and dielectric 640 membrane with a RIE process. The silicon layer 640 is then selectively wet etch removed to leave a stencil pattern as shown by the openings in the dielectric membrane 644a, 644b, 644c in Figure 29p. This sequence of processing is novel because it allows the sidewall passivation on the dielectric 640 which forms as a by-product of the RIE processing to be removed before the fragile stencil pattern is formed. The sidewall passivation cleaning requires vigorous agitation that would destroy a free standing stencil pattern. The remaining silicon layer 642 can be removed by gentle silicon selective wet etch.

Stepper Contact Printer (SCP)

Pattern generation tools made from MDI circuit membranes can be used to pattern an appropriately

sensitive resist film deposited on a substrate. MDI pattern generation tools refer to MDI circuit membrane applications such as the SLV, SPV and MLV lithographic tools, and the more conventional fixed pattern masks made on a low stress dielectric membrane with appropriate optical transmission characteristics (see above). A MDI fixed pattern mask is a single layer metallization pattern formed on a MDI dielectric membrane with one of the MDI fabrication methods presented above. A method of alignment to an existing image on a substrate through electrical inductive coupling is presented below; it is also incorporated into the MDI circuit membrane fixed pattern generation tool.

Contact printing methods are inexpensive and can provide nearly unlimited lithographic feature size imaging capability. However, the use of thick mask plates for image transfer to the resist on the substrate must come in contact with the resist to achieve the best image results. This contact is brought about by the application of strong vacuum forces that bend the rigid mask plate into conformal contact with the substrate. The result of applying such strong vacuum forces often causes small particles of the resist to adhere to the rigid mask which in turn requires the mask to be cleaned or, if undetected, prevents correct image transfer by nonconformal contact to the substrate or an imaging defect during subsequent exposures. Proximity printing is similar to contact printing except the mask is not brought into contact but is held several micrometers over the substrate called the proximity gap. The effectiveness of proximity printing to produce small feature size images is directly proportional to the size of the proximity gap. Further, contact printing has been limited to printing a complete substrate in one exposure instead of smaller portions of the substrate as is the case with conventional stepper

projection lithography equipment. The time to pull vacuum during the contact printing process is lengthy, and therefore, making several contact print exposures on a single substrate would be prohibitive in time without consideration to the compounded mask cleanliness challenge and the mechanical complexity of vacuum application to uneven or overlapping ridge mask and substrate plate during contact.

Figure 30 shows a cross-section of a stepping contact lithographic exposure equipment that combines the well known contact or proximity lithography methods with a stepper mechanical motion and the pattern generation tools and alignment means of MDI circuit membranes presented herein. The substrate (workpiece) 662 is held by a conventional vacuum chuck (not shown) and is positioned by conventional mechanical and piezoelectric motion control mechanisms (not shown). The MDI pattern generation tool 660 is held over the substrate 662 a distance "d" of less than 25 μm and rough alignment over a portion of the substrate 662 is made by conventional optical means. The center of the MDI pattern generation tool 660 is then extended by applying a small fluid pressure P of less than 100g per square cm to lower the circuit membrane into a desired proximity distance position shown by dotted line 668 or conformal contact with the substrate 662. Final precision alignment of the pattern generation tool 660 to the substrate is accomplished by the inductive coupling (electro-magnetic) means disclosed below. The low mass and elastic nature of the MDI circuit membrane allows the pattern generation tool to be rapidly brought in and out of contact with the substrate. Once an exposure is complete, the pattern generation tool is brought out of contact with the substrate and stepped (moved) under computer control to the next area on the substrate to be exposed. Also shown are circuit membrane frame 672 and a

lithography equipment fixture 676 for holding the pattern generation tool 660, 672.

Electro-Magnetic Lithographic Alignment Method

The lithographic pattern generation tools disclosed herein as the SLV, SPV, MLV, and fixed masks are capable of pattern generation with Critical Dimensions (CDs) or minimum pattern feature sizes of less than 50 nm. A fixed pattern generation tool, commonly referred to as a mask, can be made with the MDI circuit membrane process (as disclosed above) with the capability of pattern generation CDs directly proportional to the wavelength of the exposure source. Potential exposure sources are UV, DUV, E-Beam and particle beam. (Fixed masks made with the MDI process are circuit membranes of typically less than 4 μm thickness and with a single layer of patterned material to be used as in conventional lithographic masks.

Alternately, the MDI circuit membrane can be a stencil pattern, where the pattern to be generated is represented in the circuit membrane as trenches that go completely through the membrane. Fixed pattern stencil membranes are required for E-Beam or particle beam lithographic process, where the exposure source must physically pass through the mask to be imaged (patterned). Prototype particle beam stencil masks have been developed by Ion Microfabrication Systems.)

The utility of the CD generation capability of a pattern generation tool for the manufacture of ICs, however, is dependent on the ability to align or register multiple overlaying patterns. Accepted pattern alignment tolerances used presently in the semiconductor industry are typically $\pm 25\%$ of the CD value for a set of overlaying patterns.

Alignment for pattern generation with CDs of approximately 1 μm or greater can be done with optical

microscopes by overlaying or matching alignment patterns on the substrate with corresponding patterns on the surface of the pattern generation tool. The microscope can view through the pattern generation tool, since it is typically made from transparent dielectric materials.

The preferred embodiments of the SLV, SPV, and MLV are to provide the capability to generate patterns that have critical dimensions of less than 100 nm. Such patterns require alignment methods capable of achieving pattern registration of less than ± 25 nm. Optical alignment methods presently available cannot achieve such critical dimensions. The MDI pattern generation tools achieve alignment for critical dimensions of less than 100 nm through the use of electro-magnetic proximity sensing. Figure 28a shows an example of a PGT alignment coil 494. This metal coil 494 is fabricated by patterning a thin metal film (typically less than 1 μm in thickness) on the surface of the substrate being patterned (i.e., on the wafer). The placement of the coil patterns 494 on the substrate is typically along two adjoining sides of the area to be exposed or patterned. Coil patterns can also be placed within the area of the substrate to be patterned; they are not restricted to the edge or sides of the pattern area. The coil patterns are typically less than 800 μm by 100 μm . The electrode contact pads 496, 498 of the coil area 494 are typically 50 μm by 50 μm in area. A similar pattern 494 corresponding to structure 430 in Figure 24 is on the surface of the pattern generation tool membrane (not shown) plus two electrode probe points that extend down from the surface of the circuit membrane of the pattern generation tool. These pattern generation tool probe points make contact with the electrode pads associated with the substrate coil 494, and electrical signals are generated in the substrate coil 494. It should be apparent, though less convenient, that

signals can be supplied to the substrate by connections from the edge of the substrate and not directly from the pattern generation tool.

The signals from the substrate coil are sensed by the 5 corresponding alignment coil in the pattern generation tool. The pattern generation tool or the substrate are then moved in an X-Y and angular manner until predefined electrical parameter settings are achieved via the signals sensed from the substrate coil. This is possible due to 10 the close proximity of the substrate and the pattern generation tool, and the integrated control logic electronics of the pattern generation tool. Alignment sensing accuracies smaller than 10 nm can be achieved in this manner. The electrode pads of the substrate coil 15 typically have dimensions of less than 2 mils on a side, and the probe point electrodes that extend from the pattern generation tool to make contact with the substrate coil pads are typically less than 12 μm in diameter and height. A fluid pressure applied to the back side of the 20 pattern generation tool may be used to bring the surface of the pattern generation tool in near contact (proximity) or full contact with the surface of the substrate during the alignment process.

Alternately, Figure 28b shows an alignment coil 495 25 that can be placed on the substrate for alignment sensing by the pattern generation tool. A signal is induced in one side 495a of the coil by a corresponding coil in the pattern generation tool. This signal is then sensed at the other end 495b of the coil by a second coil in the 30 pattern generation tool. Alignment is achieved in the same manner as discussed above.

Inexpensive piezoelectric motion control devices are commercially available from Burleigh Instruments, Inc. (Fisher, New York) that demonstrate motion control 35 capability of less than one Angstrom; such piezoelectric

precision motion has been demonstrated in the AFM (Atomic Force Microscope) equipment where motion control of less than one Angstrom is required.

MDI Circuit Membrane Flat Panel Display

- 5 Much of the cost of manufacturing a flat panel display (without consideration for yield loss) is the cost of the substrate on which it is fabricated. The substrate must meet requirements of flatness imposed by lithography tools and high temperatures imposed by various fabrication 10 steps.
- An MDI circuit membrane flat panel display is formed on a rigid optically flat reusable substrate such as fused silica or fused quartz. Other substrates can be used to meet the requirements imposed by the fabrication 15 processing steps. A release agent such as KBr or KBO₂ is deposited onto the substrate and then a dielectric layer or layers are deposited to seal the release agent deposited film (as described above). The release agent is required to have a working temperature higher than the 20 highest temperature of the various fabrication process steps employed and be readily soluble in a solvent that is not detrimental to the finished display device. As an example, KBr has a melting point of 734°C and is readily soluble in DI water.
- 25 The flat panel display is conventionally composed of rows and columns of pixel elements which generate the gray shades or the RGB (Red, Green, Blue) colors of the display. The operation of the pixels results in the generation of the image on the display. The pixels of the 30 display can be made with conventional active matrix LCD technology. The preferred embodiment of the MDI circuit membrane display uses redundant circuit devices at each pixel and the above referenced fine grain testing technology to correct for circuit fabrication defects.

Secondly, the MDI circuit membrane display makes use of electro luminescent phosphors, similar to the phosphors used in conventional TV and industrial monitors. The phosphors are applied after the completion of the fabrication of the circuitry of the display. The display circuitry is then used in the final manufacturing process steps to cause the selective deposition of the RGB phosphors to their respective RGB electrodes.

Additionally, the multiple chip module interconnect circuit membrane technology disclosed above also is employed to bond ICs at the edges of the display panel and at any desired location on the back of the panel. The ability to attach ICs is of significant importance in lessening the complexity of the design and manufacturing of the display. ICs bonded to the back of the display do not interfere with or obscure the visual operation of the phosphor based display, because the display is not back lit as is the case with LCD displays, but generates its own luminescence.

Figure 31a shows the cross-section of a MDI circuit membrane display 700 while still attached to a reusable quartz fabrication substrate 702 with intervening release agent 703. The control logic circuit 704-1, 704-2, 704-3 for each RGB pixel has been fabricated from a-Si or polysilicon thin film transistors (TFTs), and electro-phoretic plating electrodes 708-1, 708-2, 708-3 (pads) have been formed as a final metallization process step over each RGB pixel logic circuit 704. The plating electrodes 708-1, 708-2, 708-3, one for each RGB phosphor of a pixel, can be selectively addressed and a specific plating potential applied. At the end of each row and column of pixels are bonding pads 710 for ICs (die). The ICs provide control and memory logic for turning individual pixels on or off, therefore generating a display image. It should be noted that the control and/or

memory logic 712, 713 (see Figure 31b) could also be fabricated as part of the MDI circuit membrane 700 just as the individual pixel control circuits 704-1, 704-2, 704-3 have been. This is a design/manufacturing option, and 5 would replace most or all of the bonded die. All fabrication processing steps of the MDI circuit membrane are established techniques.

Figure 31b shows in cross section the MDI circuit membrane display 700 attached to a support frame 718 and 10 released from the reusable fabrication substrate. The support frame 718 is bonded to the MDI circuit membrane 700 by an anodic method as one technique, and then the MDI circuit membrane 700 is scribed along the side of the fabrication substrate 702. This exposes the release agent 15 703 of Figure 31a. The display assembly is then placed in a solvent that activates the release agent 703, causing the display to be freed from the reusable fabrication substrate 702. Optionally, control and memory logic die 713 are attached to the display backside. These IC 713 20 connect to pixels along row or column interconnect metallization.

Figure 31c shows the display after electro-phoretic plating of the individual RGB phosphors 708-1, 708-2, 708-3. Each RGB phosphor is plated separately by 25 immersion of the display in a plating solution of a specific phosphor, and then using the control and pixel logic 704-1, 704-2, 704-3 of the display to select appropriate pixel elements (either Red or Green or Blu) and apply the desired plating electrical potential.

30 The substrate used to fabricate the flat screen display could also be a MDI membrane with a semiconductor device layer. Using a semiconductor based MDI membrane as the substrate to fabricate the flat screen display will not require any substantial difference in processing 35 steps, however, due to the limited size of available

silicon wafers (presently 8 inches) and the circular shape, the use of a semiconductor wafer as the starting substrate greatly limits the maximum size of the display.

Three Dimensional IC Structures

5 Three dimensional (3D) IC structures can be formed from MDI circuit membranes. This is a novel capability of the MDI IC membrane. The low stress dielectrics of silicon dioxide or silicon nitride can be formed to withstand working temperatures in excess of 400°C. This
10 high working temperature capability allows the use of anodic or thermal (quartz to quartz or silicon to quartz) bonding procedures that are typically high temperature processes. The dielectric circuit membranes are optically transparent and thin, allowing the circuit membranes to be
15 aligned very accurately prior to bonding. As shown in Figure 32a, the semiconductor devices 730-1, 730-2, 730-3 that are embedded in a first MDI circuit membrane 732 can have interconnect metallization 736-1, 736-2, 736-3 applied to both sides of the membrane 732 completing all
20 intra-membrane interconnections. Also shown are opposed semiconductor device gate electrodes 742-1, 742-2, 742-3. Figure 32a shows the two MDI circuit membranes or ICs 732,
25 746 prior to bonding. This allows the circuit membranes to be coated as necessary for the forming of the anodic or thermal membrane-to-membrane bond 752 of circuit membrane 732 to the second membrane 746 which includes similarly
30 semiconductor devices 748-1, 748-2, 748-3, and interconnect metallization 750-1, 750-2, 750-3. After two membranes 732, 746 are bonded as shown in Figure 32b, only vertical interconnect metallization 754-1, 754-2 can be employed to route signals from lower membrane layer 746.

MDI circuit membranes 732, 746 are aligned using established optical alignment mark techniques and anodically or thermally bonded 752 to each other. The

circuit membranes 732, 746 that are anodically or thermally bonded are complete of all necessary semiconductor device processing steps, and only require the completion of vertical interconnect metallization 5 754-1, 754-2. The final interconnect metallization 754-1, 754-2 is completed by etching vias 756-1, 756-2 through the last circuit membrane 732 to be bonded to electrical contacts on the circuit membrane 746 onto which it was bonded. Well known metal deposition and patterning 10 process steps are applied. If additional circuit membrane ICs are to be bonded to a 3D IC structure, a dielectric coating is applied to the 3D structure to isolate any metallization as a necessary requirement to a subsequent bonding step.

15 Anodic bonding 752 is a glass-to-glass process. The MDI circuit membranes 732, 746 are each provided with a 1 μm thick or greater final deposition of silicon dioxide to form the bond 752 prior to the anodic bonding process step. Anodic processing is well known and there are 20 numerous such techniques used in conventional glass plate manufacturing.

Thermal (fusion) bonding of silicon to quartz or glass substrates is an established technique. It can be used instead of anodic bonding methods to bond MDI circuit 25 membranes.

The ability to use optical data transmission as an interconnect means (instead of metallization interconnect) between MDI circuit membrane layers 732, 746 is a direct consequence of the method of fabricating the 3D IC 30 structure. Wave guides (not shown) between optical transceiver components can be formed from vias by bonding vias (openings) corresponding to the various optical transceiver devices on circuit membranes. The normally high transmissive nature of the circuit membranes and the 35 short layer-to-layer distances between the circuit

membranes allow integrated optical semiconductor devices to provide the communication function through vias or directly through certain dielectric materials.

Integrated circuits formed on a MDI circuit membrane 5 can be cut from the circuit membrane in much the same manner as ICs or die are presently cut from a rigid wafer substrate in order to be packaged. This is possible due to the net low stress of the circuit membrane. Figures 32c and d show die cut from a circuit membrane and bonded 10 onto a rigid substrate such as a silicon wafer, quartz, glass, metal, etc. In the case of a metal rigid substrate, dielectric and interconnect layers may be added to provide a better bonding surface for the membrane IC or to provide interconnection from bond pads on the IC to 15 bond out pads at the edge of the metal substrate. The use of a metal substrate to attach the membrane IC provides clear advantages, if not an optimal means, for thermal cooling of the IC.

Once the circuit membrane substrate or wafer is cut 20 into dice in the manner which is present practice, a pick and place bonding tool can pick up the die with slight vacuum pressure, align it over the substrate onto which it is to be bonded and bond it to the substrate. Figures 32c and d each show stocked membrane die 764-a, 764-b, 764-c 3/4" 25 bonded to a rigid substrate. Alternately, the membrane die 764-a, 764-b, 764-c can be bonded with compressive, anodic or fusion (thermal) techniques to a circuit membrane (not shown), such as a MCM interconnect circuit membrane.

30 Figure 32c shows a 3D circuit structure of membrane dice (ICs) 764-a, 764-b, 764-c bonded by compression technique to a rigid substrate 770. This is accomplished by aligning metal pads 772-1, 1,772-2, ..., 772-k, ..., 772-y² on the rigid substrate 770 and metal pads 776-1, 776-2, ..., 776-w on the membrane die 764-a, ..., 764-c 3/4" 4t

and then applying temperature and pressure (as explained previously). Also shown are bonding-out pads 778-1, 778-2. The surfaces are bonded together by the metal pads which also serve as circuit interconnect and thermal relief paths.

Figure 32d shows a 3D circuit structure of membrane dice 764-a, 764-b, 764-c bonded by anodic or fusion (thermal) techniques to a substrate 770. The handling of the individual die 764-a, 764-b, 764-c can be done in a manner similar to that described above, and the bonding and interconnect completion methods are also as described above for bonding the circuit membranes together.

The benefits of such die assembly practice are dramatically increased circuit device densities and low thermal mass for efficient cooling. The handling equipment for making such a circuit assembly is presently available.

This disclosure is illustrative and not limiting; further modifications will be apparent to one skilled in the art in light of this disclosure and the appended claims.